

高速隔离式 CAN 收发器

UMISO1050 DUB8/WSOP8/WSOP16
UMISO1052 WSOP8/WSOP16

1 描述

UMISO105x 系列是符合 ISO11898-2 标准的隔离式 CAN 收发器。该系列器件通过二氧化硅 (SiO_2) 绝缘隔离层将逻辑输入与输出缓冲器进行电气隔离, UMISO105x 宽体封装的隔离耐压高达 5000 V_{RMS} , UMISO1050 DUB8 封装的隔离耐压高达 3750 V_{RMS} , 此外, 该系列器件还具备高电磁抗扰度与低辐射特性。

UMISO105x 系列支持高达 5Mbps 的通信速率。该器件专为严苛工业环境设计, 具备串线保护、接地失效和过压保护 (-40 V 至 40 V) 功能, 共模电压范围为 -15 V 至 15 V 。UMISO105x 系列还具备热关断保护及驱动器显性超时功能。

UMISO1050 系列可提供 DUB8 封装、宽体 WSOP8 封装及宽体 WSOP16 封装, UMISO1052 系列可提供宽体 WSOP8 封装及宽体 WSOP16 封装, 该系列器件工作环境温度范围为 $-40\text{ }^{\circ}\text{C}$ 至 $125\text{ }^{\circ}\text{C}$ 。

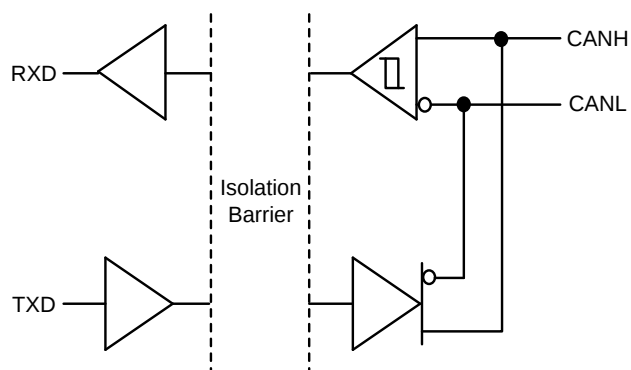
2 特性

- 完全符合 ISO11898-2 标准
- I/O 电压范围支持 3.3V 和 5V 微处理器
- 数据速率: 高达 5Mbps
- 低环路延迟: $<120\text{ ns}$ (典型值)
- 集成保护提升系统鲁棒性
 - 高达 5000 V_{RMS} 隔离电压 (宽体封装),
高达 3750 V_{RMS} 隔离电压 (DUB 封装)
 - CMTI: $\pm 200\text{ kV}/\mu\text{s}$ (典型值)
 - 长使用寿命: >40 年
 - 驱动器 (TXD) 显性超时
 - 总线故障保护: -40 V 至 $+40\text{ V}$
 - 过流和过温保护
- 符合安全规范
 - DIN EN IEC 60747-17 (VDE 0884-17)
 - UL1577
 - IEC 61010-1 和 GB 4943.1-2022
- 工作环境温度范围: $-40\text{ }^{\circ}\text{C}$ 至 $125\text{ }^{\circ}\text{C}$
- 采用 DUB8、WSOP8 和 WSOP16 封装

3 应用

- 工业自动化
- HVAC 自动化
- 光伏逆变器
- 医疗
- 电机控制
- 电信

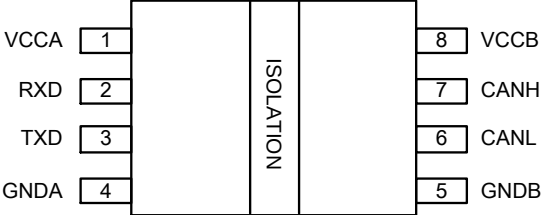
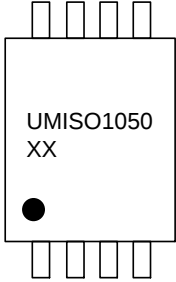
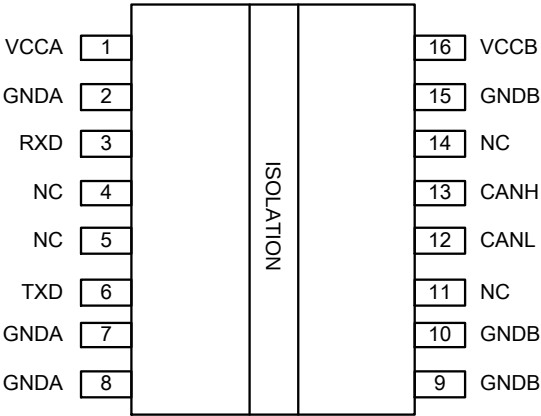
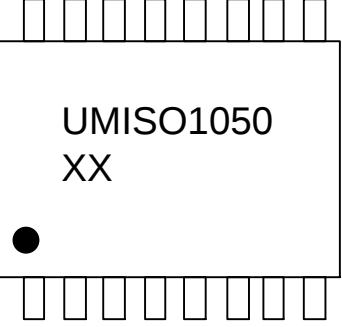
4 Simplified Channel Structure



5 Ordering Information

Part Number	Marking Code	Isolation Rating (V _{RMS})	Package Type	Shipping Qty
UMISO1050Z8	UMISO1050	3750	DUB8	800pcs/13Inch Tape & Reel
UMISO1050WS8	ISO1050	5000	WSOP8	1000pcs/13Inch Tape & Reel
UMISO1050WSG	UMISO1050	5000	WSOP16	1500pcs/13Inch Tape & Reel
UMISO1052WS8	ISO1052	5000	WSOP8	1000pcs/13Inch Tape & Reel
UMISO1052WSG	UMISO1052	5000	WSOP16	1500pcs/13Inch Tape & Reel

6 Pin Configuration and Function

 Diagram showing pin configuration for 8-pin package. The chip is divided into three sections: VCCA (pins 1-4), ISOLATION (pins 5-6), and VCCB (pins 7-8). Pin 1 is VCCA, Pin 2 is RXD, Pin 3 is TXD, Pin 4 is GNDA, Pin 5 is GNDB, Pin 6 is CANL, Pin 7 is CANH, and Pin 8 is VCCB.	 UMISO1050 XX XX: Week Code UMISO1050Z8 DUB8
 Diagram showing pin configuration for 16-pin package. The chip is divided into three sections: VCCA (pins 1-4), ISOLATION (pins 5-6), and VCCB (pins 7-8). Pin 1 is VCCA, Pin 2 is GNDA, Pin 3 is RXD, Pin 4 is NC, Pin 5 is NC, Pin 6 is TXD, Pin 7 is GNDA, Pin 8 is GNDA, Pin 9 is GNDB, Pin 10 is GNDB, Pin 11 is NC, Pin 12 is CANL, Pin 13 is CANH, Pin 14 is NC, Pin 15 is GNDB, and Pin 16 is VCCB.	 UMISO1050 XX XX: Week Code UMISO1050WSG WSOP16

6 Pin Configuration and Function (continued)

Table 6-1. Pin Functions of UMISO1050

Pin No.			Pin Name	Function
DUB8	WSOP8	WSOP16		
1	1	1	VCCA	Power supply for isolator Logic side.
4	4	2, 7, 8	GNDA	Ground reference for isolator Logic side.
2	2	3	RXD	Receive data output.
-	-	4, 5, 11, 14	NC	Not connected.
3	3	6	TXD	Transmit data input.
5	5	9, 10, 15	GNDB	Ground reference for isolator Bus side.
6	6	12	CANL	Low-level CAN bus line.
7	7	13	CANH	High-level CAN bus line.
8	8	16	VCCB	Power supply for isolator Bus side.

6 Pin Configuration and Function (continued)

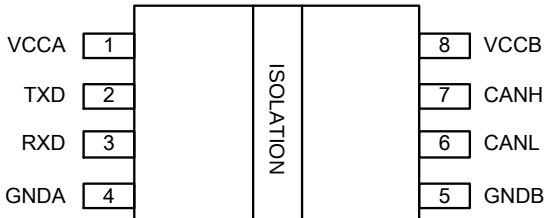
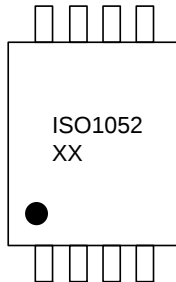
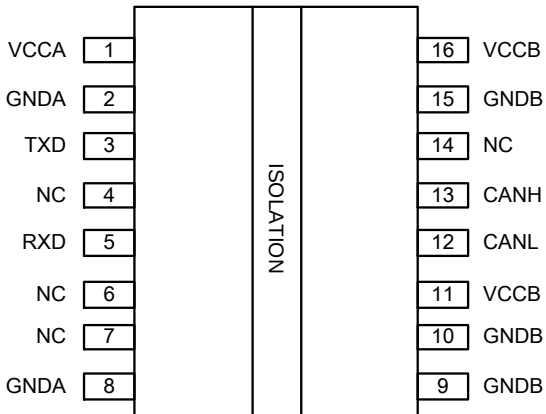
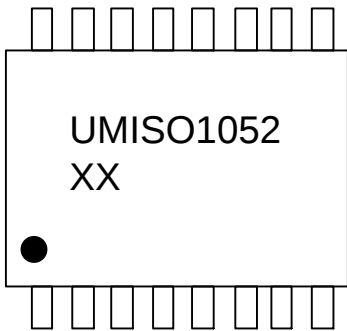
	 XX: Week Code UMISO1052WS8 WSOP8
	 XX: Week Code UMISO1052WSG WSOP16

Table 6-2. Pin Functions of UMISO1052

Pin No.		Pin Name	Function
WSOP8	WSOP16		
1	1	VCCA	Power supply for isolator Logic side.
4	2, 8	GNDA	Ground reference for isolator Logic side.
3	5	RXD	Receive data output.
-	4, 6, 7, 14	NC	Not connected.
2	3	TXD	Transmit data input.
5	9, 10, 15	GNDB	Ground reference for isolator Bus side.
6	12	CANL	Low-level CAN bus line.
7	13	CANH	High-level CAN bus line.
8	11, 16	VCCB	Power supply for isolator Bus side.

7 Specifications

7.1 Absolute Maximum Ratings (Note 1, 2)

Symbol	Parameter		Min	Typ	Max	Unit
V _{CCA}	Power supply for isolator Logic side		-0.5		+6	V
V _{CCB}	Power supply for isolator Bus side		-0.5		+6	V
V _{BUS}	Voltage range on CANH, CANL		-40		+40	V
V _{DIF}	Voltage range between CANH and CANL		-40		+40	V
V _I	Voltage range on TXD (Note 3)		-0.5		V _{CCA} +0.5	V
V _O	Voltage range on RXD (Note 3)		-0.5		V _{CCA} +0.5	V
V _{ESD}	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	All pins		±8		kV
	Contact discharge, per IEC 61000-4-2	Bus terminals to GNDB		±8		kV
I _{LU}	Latch up, per JEDEC JESD78			200		mA
T _J	Junction temperature				150	°C
T _{STG}	Storage temperature		-65		150	°C

Note 1: Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

Note 2: All voltage values, except differential I/O bus voltages, are with respect to ground terminal.

Note 3: Maximum voltage must not exceed 6 V

7.2 Recommended Operating Conditions

Symbol	Parameter		Min	Typ	Max	Unit
V _{CCA}	Power supply for isolator Logic side		2.375		5.5	V
V _{CCB}	Power supply for isolator Bus side		4.5		5.5	V
V _{IH}	Input High Voltage		2			V
V _{IL}	Input Low Voltage				0.8	V
T _A	Ambient temperature		-40		125	°C

7.3 Thermal Information

Symbol	Parameter		Value		Unit
R _{θJA}	Junction to ambient thermal resistance	DUB8	70		°C/W
		WSOP8	105		°C/W
		WSOP16	82		°C/W

7.4 Insulation Specifications

Symbol	Parameter	Conditions	Value		Unit
			DUB8	WSOP8/WSOP16	
CLR	External clearance	Shortest terminal-to-terminal distance through air	6.1	8	mm
CPG	External creepage	Shortest terminal-to-terminal distance across the package surface	6.8	8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	16	16	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>600	>600	V
	Material group	Per IEC 60664-1	I	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 150 V _{RMS}	I-IV	I-IV	
		Rated mains voltage ≤ 300 V _{RMS}	I-III	I-IV	
		Rated mains voltage ≤ 600 V _{RMS}	N/A	I-IV	
		Rated mains voltage ≤ 1000 V _{RMS}	N/A	I-II	
DIN V VDE V 0884-17:2021-10 (Note 1)					
V _{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	637	1414	V _{PK}
V _{IOWM}	Maximum operating isolation voltage	AC voltage; time-dependent dielectric breakdown (TDDB) test	450	1000	V _{RMS}
		DC voltage	637	1414	V _{DC}
V _{IOTM}	Maximum transient isolation voltage	V _{TEST} = V _{IOTM} , t = 60 s (certified); V _{TEST} = 1.2 × V _{IOTM} , t = 1 s (100% product test)	5300	7070	V _{PK}
V _{IMP}	Maximum impulse voltage	Tested in air, 1.2/50 μs waveform per IEC 62368-1,	5000	6000	V _{PK}
V _{IOSM}	Maximum surge isolation voltage	V _{IOSM} ≥ 1.3 × V _{IMP} ; Tested in oil (qualification test), 1.2/50 μs waveform per IEC 62368-1	6500	8000	V _{PK}

7.4 Insulation Specifications (Continued)

Symbol	Parameter	Conditions	Value		Unit
			DUB8	WSOP8/WSOP16	
q _{pd}	Apparent charge (Note 2)	Method a, after input/output safety test of the subgroup 2/3, $V_{ini} = V_{IOTM}$, $t_{ini} = 60$ s; $V_{pd(m)} = 1.2 \times V_{IORM}$, $t_m = 10$ s	≤5	≤5	pC
		Method a, after environmental test of the subgroup 1, $V_{ini} = V_{IOTM}$, $t_{ini} = 60$ s; $V_{pd(m)} = 1.3 \times V_{IORM}$, $t_m = 10$ s	≤5	≤5	pC
		Method b, at routine test (100% production test) and preconditioning (type test) $V_{ini} = 1.2 \times V_{IOTM}$, $t_{ini} = 1$ s; $V_{pd(m)} = 1.5 \times V_{IORM}$, $t_m = 1$ s (method b1) or $V_{pd(m)} = V_{ini}$, $t_m = t_{ini}$ (method b2)	≤5	≤5	pC
C _{IO}	Barrier capacitance, input to output (Note 3)	$V_{IO} = 0.4 \times \sin(2\pi ft)$, $f = 1$ MHz	~1.0	~1.0	pF
R _{IO}	Isolation resistance (Note 3)	$V_{IO} = 500$ V, $T_A = 25$ °C	>10 ¹²	>10 ¹²	Ω
		$V_{IO} = 500$ V, 100 °C ≤ T_A ≤ 125 °C	>10 ¹¹	>10 ¹¹	
		$V_{IO} = 500$ V at $T_S = 150$ °C	>10 ⁹	>10 ⁹	
	Pollution degree		2	2	
UL 1577					
V _{ISO}	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$, $t = 60$ s(qualification) $V_{TEST} = 1.2 \times V_{ISO}$, $t = 1$ s (100% production test)	3750	5000	V _{RMS}

Note 1: This coupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

Note 2: The characterization charge is discharging charge (pd) caused by partial discharge.

Note 3: Capacitance and resistance are measured with all pins on field-side and logic-side tied together.

7.5 Electrical Characteristics

7.5.1 Electrical Characteristics (Static)

$T_J = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$, $V_{CCA} = 2.375\text{ V}$ to 5.5 V , $V_{CCB} = 4.5\text{ V}$ to 5.5 V , $R_L = 60\Omega$, $C_L = 100\text{pF}$ (unless otherwise noted). Typical values are at $V_{CCA} = 3.3\text{ V}$, $V_{CCB} = 5\text{ V}$, $T_A = 25^{\circ}\text{C}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power supply						
I_{CCA}	Supply current logic side	$V_I = V_{CCA}$, $V_{CCA} = 5.0\text{ V}$		2.3	5	mA
I_{CCA}	Supply current logic side	$V_I = 0\text{ V}$, $V_{CCA} = 5.0\text{ V}$		4.6	8	mA
I_{CCB}	Supply current bus side	$V_I = 0\text{ V}$, bus dominant, $R_L = 60\Omega$		55	73	mA
I_{CCB}	Supply current bus side	$V_I = V_{CCA}$		3.9	12	mA
$V_{CCA(UVLO)RIS}$	Rising under voltage detection, V_{CCA}		2	2.2	2.35	V
$V_{CCA(UVLO)FAL}$	Falling under voltage detection, V_{CCA}		1.98	2.1	2.21	V
$V_{CCB(UVLO)RIS}$	Rising under voltage detection, V_{CCB}		3.7	4.0	4.3	V
$V_{CCB(UVLO)FAL}$	Falling under voltage detection, V_{CCB}		3.5	3.85	4.25	V
CAN transmit data input; pin TXD						
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{IH}	High-level input current	$TXD = V_{CCA}$			10	uA
I_{IL}	Low-level input current	$TXD = 0\text{ V}$	-10			uA
C_I	Input capacitance			5	10	pF
CAN receive data output; pin RXD						
V_{OH}	High level output voltage with $V_{CCA} = 5\text{ V}$	$I_{OH} = -4\text{mA}$, see figure 8-6	$V_{CCA} - 0.8$	4.8		V
		$I_{OH} = -20\text{uA}$, see figure 8-6	$V_{CCA} - 0.1$	5		V
V_{OH}	High level output voltage with $V_{CCA} = 3.3\text{ V}$	$I_{OH} = -4\text{mA}$, see figure 8-6	$V_{CCA} - 0.8$	3.1		V
		$I_{OH} = -20\text{uA}$, see figure 8-6	$V_{CCA} - 0.1$	3.3		V
V_{OL}	Low level output voltage	$I_{OL} = 4\text{mA}$, see figure 8-6		0.2	0.4	V
		$I_{OL} = 20\text{uA}$, see figure 8-6		0	0.1	V

7.5.1 Electrical Characteristics (Static)---continued

$T_J = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$, $V_{CCA} = 2.375\text{ V}$ to 5.5 V , $V_{CCB} = 4.5\text{ V}$ to 5.5 V , $R_L = 60\Omega$, $C_L = 100\text{pF}$ (unless otherwise noted). Typical values are at $V_{CCA} = 3.3\text{ V}$, $V_{CCB} = 5\text{ V}$, $T_A = 25^{\circ}\text{C}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Driver						
$V_{O(DOM)}$	Dominant output voltage	TXD = 0 V; $t < t_{DIO(TXD)}$; $R_L = 60\Omega$; pin CANH, see figure 8-1 and 8-2	2.75	3.5	4.5	V
		TXD = 0 V; $t < t_{DIO(TXD)}$; $R_L = 60\Omega$; pin CANL, see figure 8-1 and 8-2	0.5	1.5	2.25	V
$V_{OD(DOM)}$	Dominant differential output voltage	TXD = 0V; $t < t_{DIO(TXD)}$; $50\Omega \leq R_L \leq 65\Omega$, see figure 8-1 and 8-2	1.5		3	V
		TXD = 0V; $t < t_{DIO(TXD)}$; $45\Omega \leq R_L \leq 70\Omega$, see figure 8-1 and 8-2	1.4		3.3	V
		TXD = 0V; $t < t_{DIO(TXD)}$; $R_L = 2240\Omega$, see figure 8-1 and 8-2	1.5		5	V
$V_{O(REC)}$	Recessive output voltage	TXD = V_{CCA} ; $R_L = 60\Omega$, see figure 8-1 and 8-2	2	$0.5V_{CCB}$	3	V
$V_{OD(REC)}$	Recessive differential output voltage	TXD = V_{CCA} ; $R_L = \text{open}$	-100		100	mV
		TXD = V_{CCA} ; $R_L = 60\Omega$, see figure 8-1 and 8-2	-50		50	mV
$V_{OC(DOM)}$	Common-mode output voltage (Dominant)	See figure 8-7	2	2.5	3	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	See figure 8-7		0.3		V
$I_{OS(DOM)}$	Dominant short-circuit output current	TXD = 0 V; CANH = -15 V to 40 V; CANL = open	-100	-75		mA
		TXD = 0 V; CANL = -15 V to 40 V; CANH = open		75	100	mA
$I_{OS(REC)}$	Recessive short-circuit output current	TXD = V_{CCA} ; $-27\text{ V} \leq \text{CANH} = \text{CANL} \leq 32\text{ V}$	-5		5	mA

7.5.1 Electrical Characteristics (Static)---continued

$T_J = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$, $V_{CCA} = 2.375\text{ V}$ to 5.5 V , $V_{CCB} = 4.5\text{ V}$ to 5.5 V , $R_L = 60\Omega$, $C_L = 100\text{pF}$ (unless otherwise noted). Typical values are at $V_{CCA} = 3.3\text{ V}$, $V_{CCB} = 5\text{ V}$, $T_A = 25^{\circ}\text{C}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Receiver						
V_{TH}	Differential receiver threshold voltage	$-15\text{ V} \leq \text{CANH}, \text{CANL} \leq 15\text{ V}$	0.5		0.9	V
$V_{ID(DOM)}$	Receiver dominant voltage	$-15\text{ V} \leq \text{CANH}, \text{CANL} \leq 15\text{ V}$	0.9		9	V
$V_{ID(REC)}$	Receiver recessive voltage	$-15\text{ V} \leq \text{CANH}, \text{CANL} \leq 15\text{ V}$	-4		0.5	V
V_{HYS}	Differential receiver hysteresis voltage	$-15\text{ V} \leq \text{CANH}, \text{CANL} \leq 15\text{ V}$	50		300	mV
R_I	Input resistance	$\text{TXD} = V_{CCA}$;	15	30	40	$\text{k}\Omega$
ΔR_I	Input resistance deviation, $[1 - (R_{IN(CANH)} / R_{IN(CANL)})] \times 100\%$	$\text{TXD} = V_{CCA}$;	-3		3	%
R_{ID}	Differential input resistance	$\text{TXD} = V_{CCA}$;	30	60	80	$\text{k}\Omega$
C_{IN}	Common-mode input capacitance to ground				20	pF
C_{ID}	Differential input capacitance				10	pF
CMTI	Common-mode transient immunity	$V_I = V_{CCA}$ or 0 V , $V_{CM} = 1200\text{ V}$, see figure 8-12	150	200		$\text{kV}/\mu\text{s}$
Thermal Protection						
$T_{J(SD)}$	Thermal shutdown threshold	Temperature rising		185		$^{\circ}\text{C}$

7.5.2 Electrical Characteristics (Dynamic)

$T_J = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$, $V_{CCA} = 2.375\text{ V}$ to 5.5 V , $V_{CCB} = 4.5\text{ V}$ to 5.5 V , $R_L = 60\Omega$, $C_L = 100\text{pF}$ (unless otherwise noted). Typical values are at $V_{CCA} = 3.3\text{ V}$, $V_{CCB} = 5\text{ V}$, $T_A = 25^{\circ}\text{C}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Device switching characteristics						
t _{PROP(LOOP1)}	Total loop delay, driver input TXD to receiver RXD, recessive to dominant	See figure 8-8	90	120	210	ns
t _{PROP(LOOP2)}	Total loop delay, driver input TXD to receiver RXD, dominant to recessive	See figure 8-8	90	120	210	ns
Driver switching characteristics						
t _{PLH}	Propagation delay time, recessive to dominant output	See figure 8-4		53	110	ns
t _{PHL}	Propagation delay time, dominant to recessive output			55	110	ns
t _R	Differential output signal rise time			28	50	ns
t _F	Differential output signal fall time			30	63	ns
t _{DTO(TXD)}	TXD dominant time-out time	C _L = 100pF, see figure 8-9	0.8	2.6	6.5	ms
Receiver switching characteristics						
t _{PLH}	Propagation delay time, low to high level output	See figure 8-6	66	80	130	ns
t _{PHL}	Propagation delay time, high to low level output		51	77	105	ns
t _R	Output signal rise time(RXD)			2.6	6	ns
t _F	Output signal rise time(RXD)			2	6	ns
FD timing parameters, see figure 8-11						
t _{BIT(BUS)}	Transmitted recessive bit width	t _{BIT(TXD)} = 500ns	435		530	ns
		t _{BIT(TXD)} = 200ns	155		210	ns
t _{BIT(RXD)}	Bit time on pin RXD	t _{BIT(TXD)} = 500ns	400		550	ns
		t _{BIT(TXD)} = 200ns	120		220	ns
Δt _{REC}	Receiver timing symmetry	t _{BIT(TXD)} = 500ns	-65		40	ns
		t _{BIT(TXD)} = 200ns	-45		15	ns

8 Parameter Measurement Information

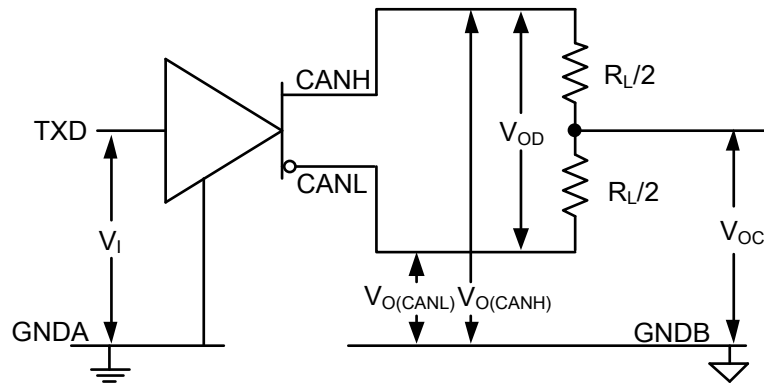


Figure 8-1. Driver Voltage, Current and Test Definitions

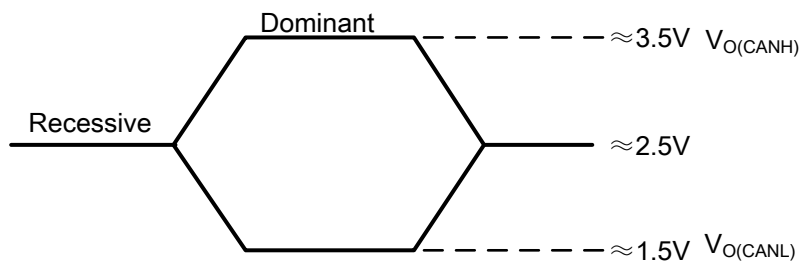


Figure 8-2. Bus Logic State Voltage Definitions

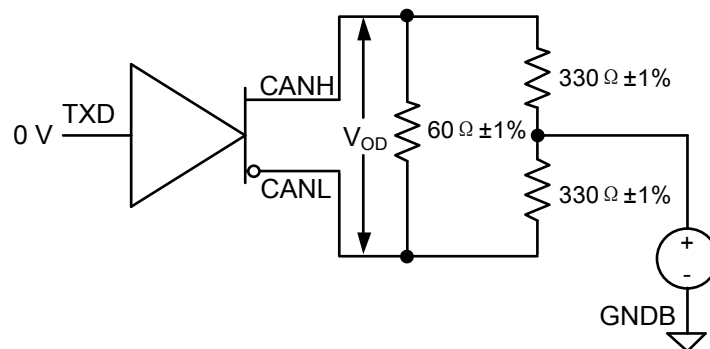
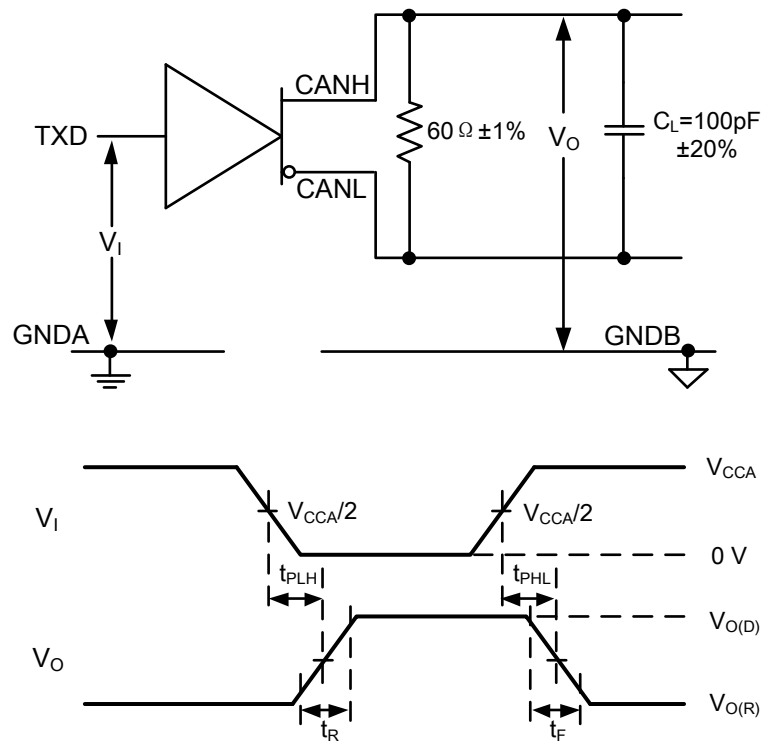


Figure 8-3. Driver V_{OD} With Common-Mode Loading Test Circuit

8 Parameter Measurement Information (continued)



Note 1: The input pulse is supplied by a generator having the following characteristics: PRR≤125 kHz, 50% duty cycle, $t_R \leq 6$ ns, $t_F \leq 6$ ns, $Z_O = 50 \Omega$.

Note 2: C_L includes instrumentation and fixture capacitance within $\pm 20\%$.

Figure 8-4. Driver Test Circuit and Voltage Waveforms

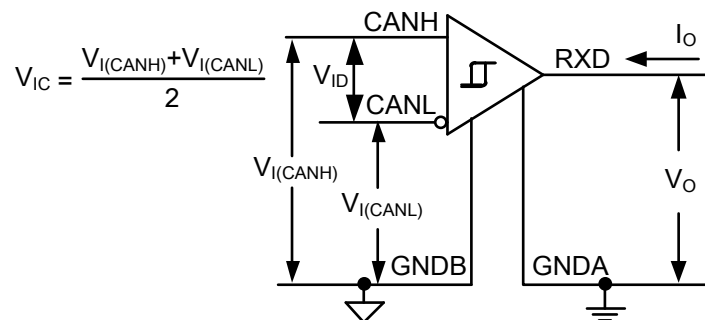
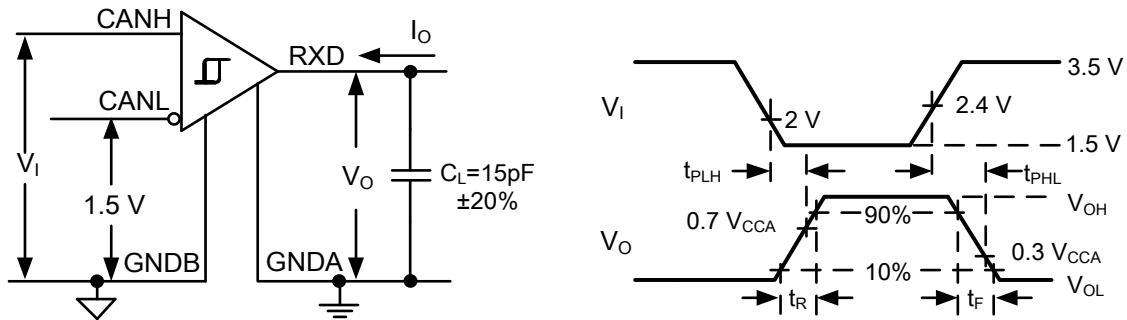


Figure 8-5. Receiver Voltage and Current Definitions

8 Parameter Measurement Information (continued)



Note 1: The input pulse is supplied by a generator having the following characteristics: $PRR \leq 125 \text{ kHz}$, 50% duty cycle, $t_R \leq 6 \text{ ns}$, $t_F \leq 6 \text{ ns}$, $Z_0 = 50 \Omega$.

Note 2: C_L includes instrumentation and fixture capacitance within $\pm 20\%$.

Figure 8-6. Receiver Test Circuit and Voltage Waveforms

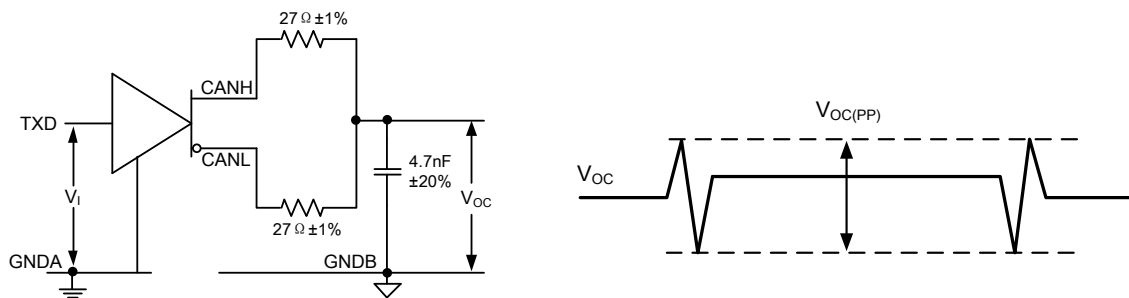


Figure 8-7. Peak-to-Peak Output Voltage Test Circuit and Waveform

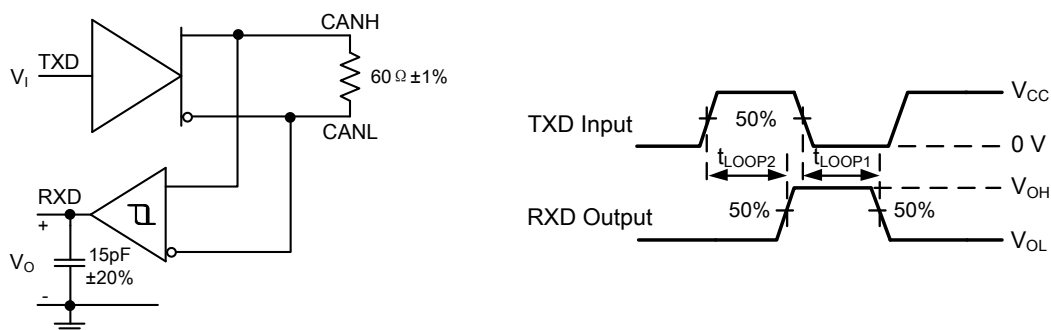


Figure 8-8. t_{LOOP} Test Circuit and Voltage Waveforms

8 Parameter Measurement Information (continued)

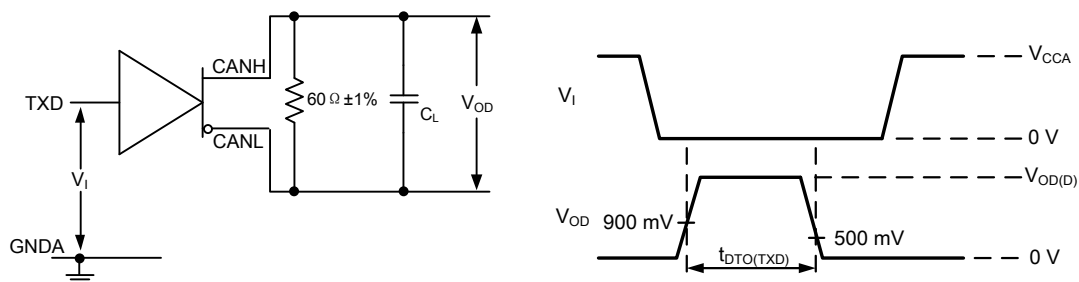


Figure 8-9. Dominant Time-out Test Circuit and Voltage Waveforms

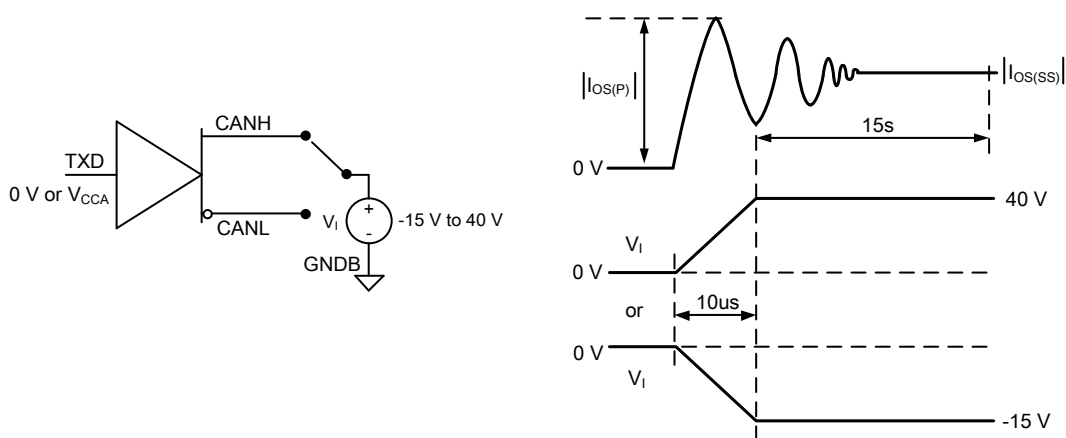


Figure 8-10. Driver Short-Circuit Current Test Circuit and Waveforms

8 Parameter Measurement Information (continued)

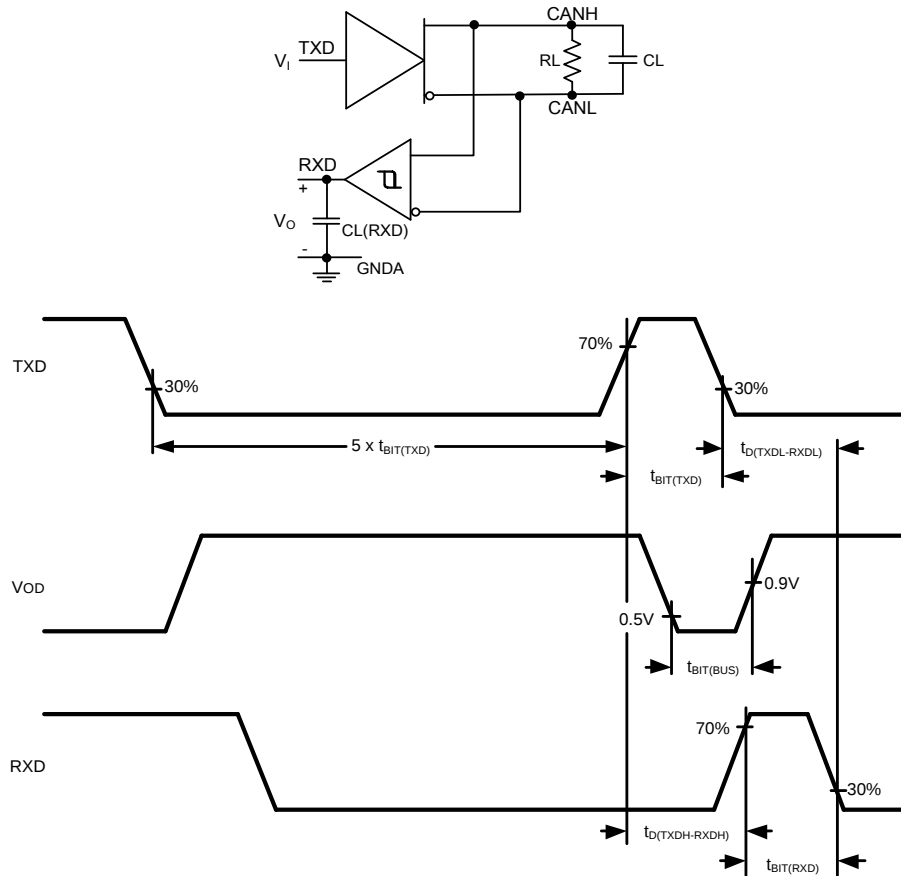
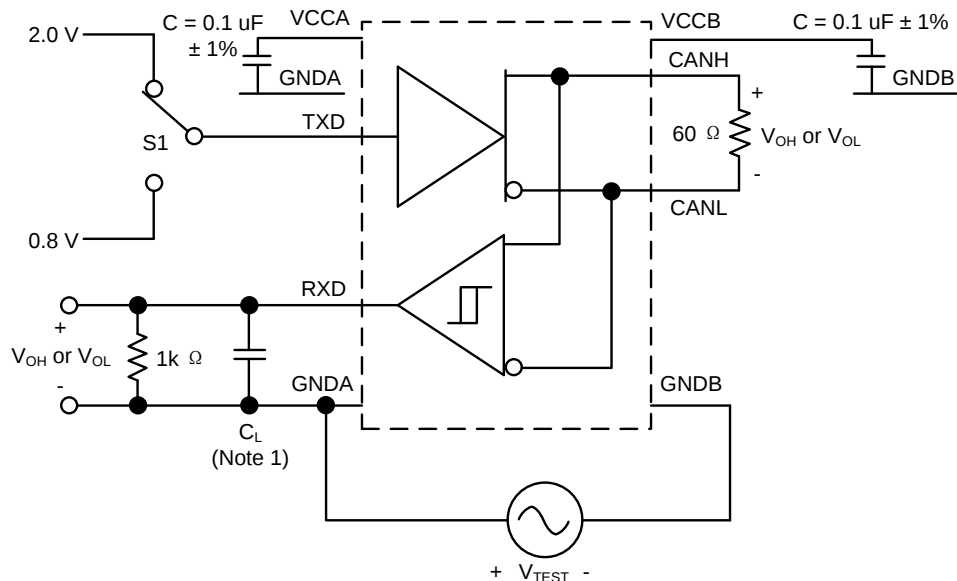


Figure 8-11. CAN FD Timing Parameter Measurement



Note 1: C_L includes probe and jig capacitance.

Figure 8-12. Common-Mode Transient Immunity Test Circuit

9 Detailed Description

9.1 Overview

The UMISO105x isolated CAN transceivers series provide galvanic isolation of up to 3750 V_{RMS} (DUB8 package) and up to 5000 V_{RMS} (WSOP8/WSOP16 package), and which is fully compatible with the ISO11898-2 standard. Additionally, the devices can achieve efficient and stable communication across isolation barrier with 200kV/ μ s CMTI and up to 5 Mbps data rate. The logic side power supply is 2.375V to 5.5V which makes the devices ideal for communication with the microcontroller in applications like solar inters, motor control and HVAC systems. The devices are designed for operation in especially harsh environments that feature cross-wire, overvoltage and loss of ground protection from -40 V to 40 V, as well as -15V to 15V common-mode range. The UMISO105x series also feature thermal protection and transmit data dominant time out function.

9.2 CAN Bus States

The CAN bus has two states during operation: dominant and recessive. A dominant bus state, equivalent to logic low, is when the bus is driven differentially by a driver. A recessive bus state, equivalent to a logic high, is when the bus is biased to a common mode of $V_{CCB}/2$. The host microprocessor of the CAN node will transmit and receive data via the bus lines CANH and CANL. The differential receiver converts the analog data on the bus lines into digital data which is output to pin RXD.

9.3 Device Functional Modes

Table 9-1. Driver Function Table (Note 1)

V _{CCA}	V _{CCB}	Input	TXD Low-Level Time	Outputs		Bus State
		TXD		CANH	CANL	
Power On	Power On	L	< t _{DTO(TXD)}	H	L	Dominant state
		L	> t _{DTO(TXD)}	V _{CCB} /2	V _{CCB} /2	Recessive state
		H or Open	X	V _{CCB} /2	V _{CCB} /2	Recessive state
Power On	Power Down	X	X	Z	Z	Z
Power Down	Power On	X	X	V _{CCB} /2	V _{CCB} /2	Recessive state

Note 1: X = Don't care, Z = high impedance.

Table 9-2. Receiver Function Table (Note 1)

V _{ID} = V _{CANH} - V _{CANL}	Bus State	RXD
V _{ID} ≥ 0.9V	Dominant state	L
0.5V < V _{ID} < 0.9V	Indeterminate	Indeterminate
V _{ID} ≤ 0.5V	Recessive state	H
Open	Open	H

Note 1: X = Don't care, Z = high impedance.

9.4 Fail-Safe Features

9.4.1 TXD dominant time-out function

A ‘TXD dominant time-out’ timer is started when pin TXD is set LOW. If the LOW state on pin TXD persists for longer than $t_{DIO(TXD)}$, the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when pin TXD is set HIGH.

9.4.2 Overtemperature protection

The output drivers are protected against overtemperature conditions. If the operating junction temperature exceeds the shutdown junction temperature, $T_{J(SD)}$, the output drivers will be disabled until the operating junction temperature falls below $T_{J(SD)}$ and TXD becomes recessive again. Including the TXD condition ensures that output driver oscillations due to temperature drift are avoided.

10 Application Information

10.1 Typical Application

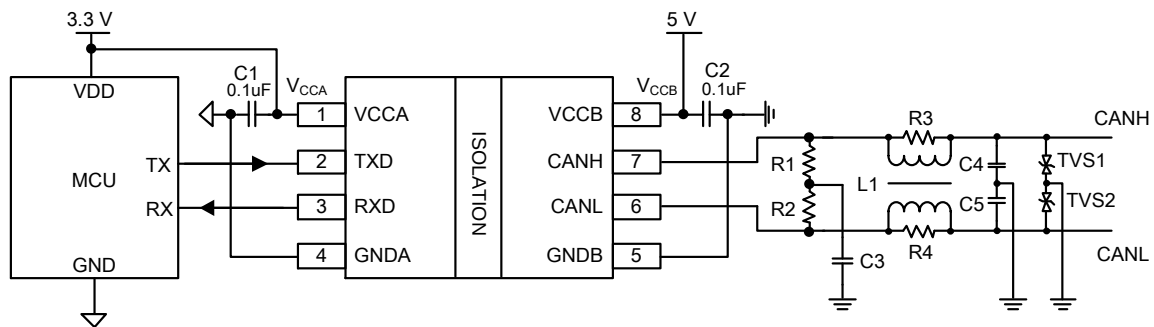
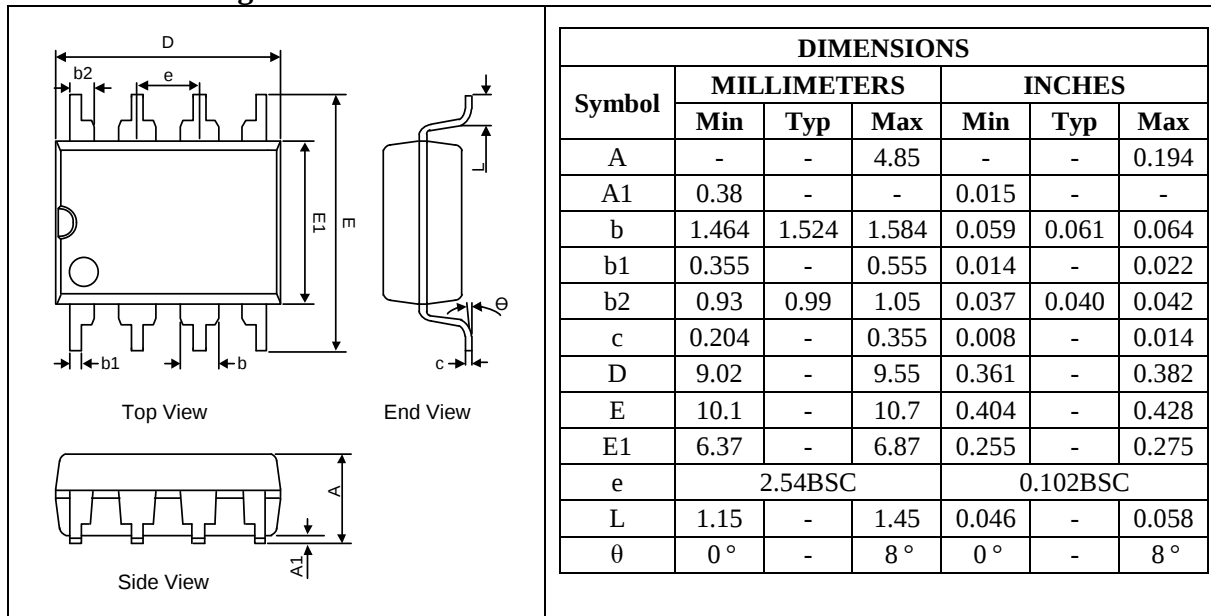


Figure 10-1. UMISO1052 Application Circuit

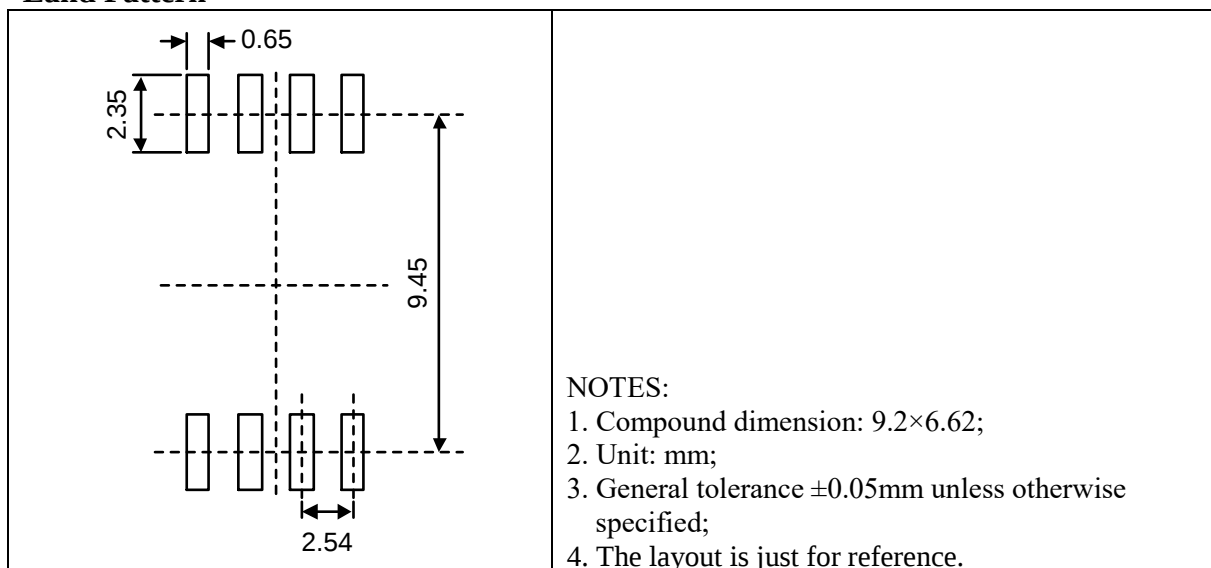
Package Information

DUB8

Outline Drawing

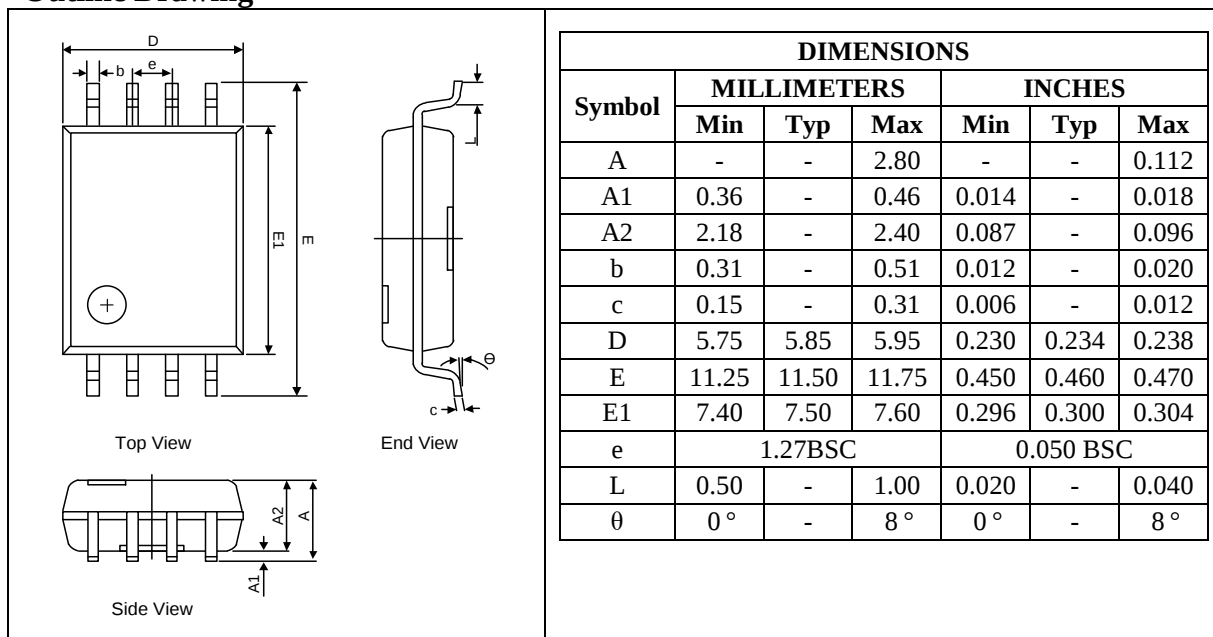


Land Pattern

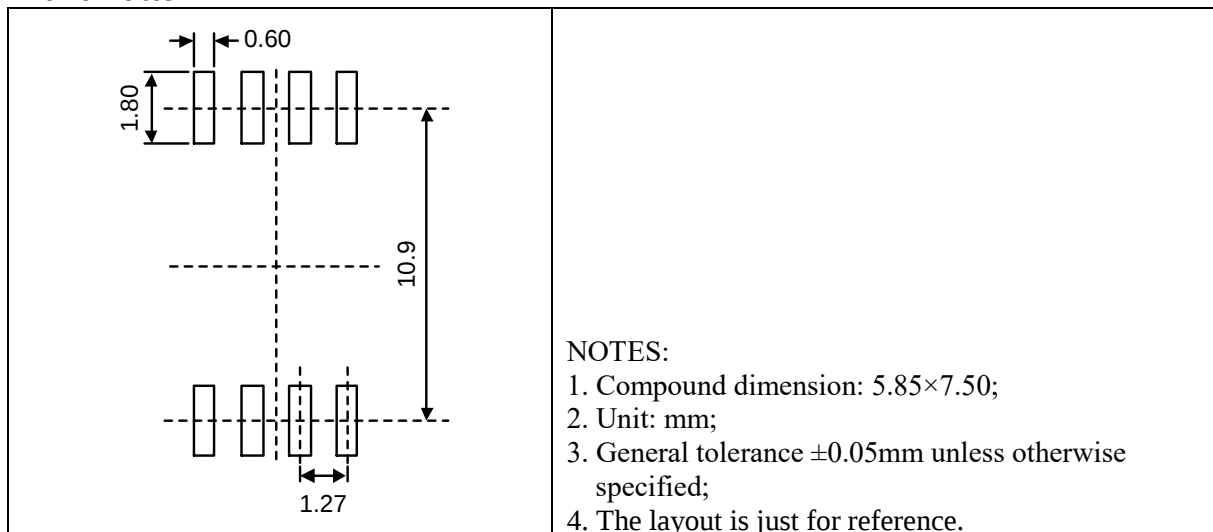


WSOP8

Outline Drawing

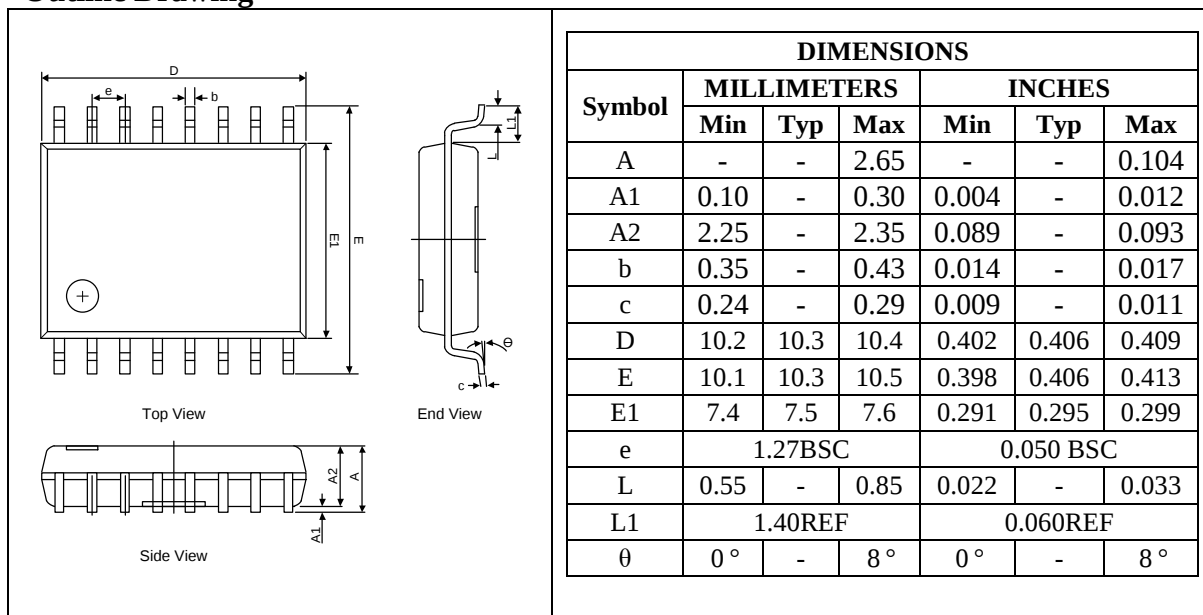


Land Pattern

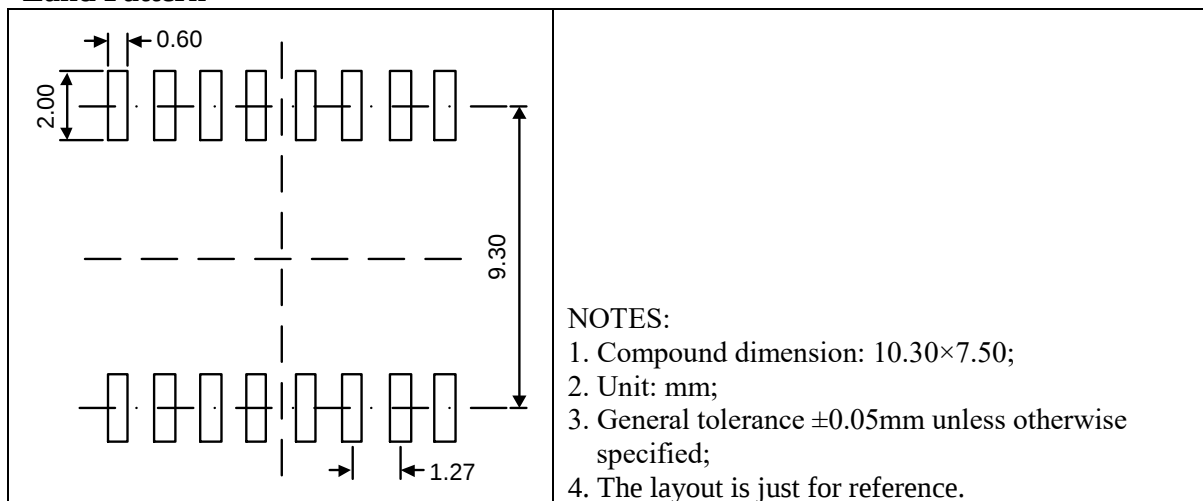


WSOP16

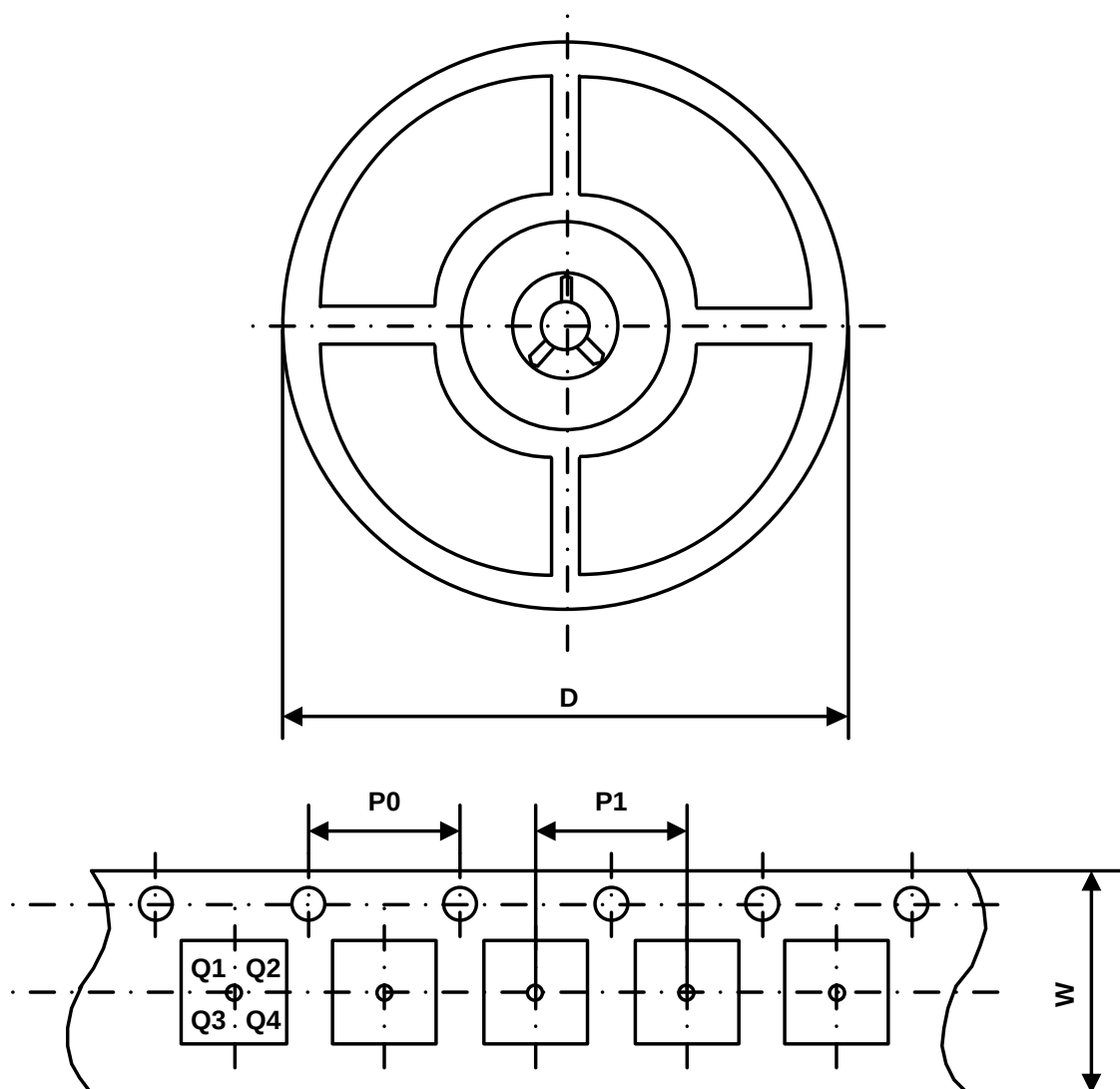
Outline Drawing



Land Pattern



Packing Information



Part Number	Package Type	Carrier Width (W)	Pitch (P0)	Pitch (P1)	Reel Size (D)	PIN 1 Quadrant
UMISO1050Z8	DUB8	24 mm	4 mm	16 mm	330 mm	Q1
UMISO1050WS8	WSOP8	16 mm	4 mm	16 mm	330 mm	Q1
UMISO1050WSG	WSOP16	16 mm	4 mm	12 mm	330 mm	Q1
UMISO1052WS8	WSOP8	16 mm	4 mm	16 mm	330 mm	Q1
UMISO1052WSG	WSOP16	16 mm	4 mm	12 mm	330 mm	Q1

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