具有待机模式的高速 CAN 收发器

UMCAN1044VS8 *SOP8*
UMCAN1044NS8 *SOP8*
UMCAN1044VDA *DFN8 3.0×3.0*
UMCAN1044NDA *DFN8 3.0×3.0*

1 描述

UMCAN1044 是高速 CAN 收发器，可在控制器局域网（CAN）协议控制器和物理双线式 CAN 总线之间提供接口。该收发器专用于汽车业的高速 CAN 应用，可以为微控制器中的 CAN 协议控制器提供发送和接收差分信号的功能。

UMCAN1044 具备针对 12V 汽车应用优化的功能特性和出色的电磁兼容性 (EMC) 性能。此外，UMCAN1044 还具有以下特点：

- 电源关闭时，CAN总线具有良好的无源性能
- 具有总线唤醒功能的超低电流待机模式
- 即使不使用共模扼流圈，也具有出色的电磁兼容（EMC）性能
- 带有V_{IO} 管脚的型号可直接连接电源电压为3.3V和5V的微控制器

UMCAN1044实现了ISO 11898-2:2024和SAE J2284-1至SAE J2284-5中定义CAN物理层。可在CAN FD快速相位下，以高达5 Mbit/s的数据传输速率进行可靠通信。在简单的拓扑网络中，速率可高达8 Mbit/s。这些特性使UMCAN1044成为各类高速CAN网络的理想选择，特别是需要通过总线实现唤醒功能的待机模式的节点。

2 应用

- 汽车工业中的高速 CAN 应用
- 基础设施和农业设备
- 电梯
- 联网的传感器/执行器

3 特性

- 完全符合ISO 11898-2:2024、SAE J2284-1至SAE J2284-5和SAE J1939-14标准
- 电源电压范围：4.5V至5.5V
- V_{IO}电压范围：2.9V至5.5V
- 超低电流待机模式，具有本地和总线唤醒功能
- 针对 12 V 汽车系统的应用进行了优化
- 低电磁辐射(EME)和高电磁抗扰度(EMI)，符合拟议的EMC标准IEC 62228-3和SAE J2962-2标准
- 在较简单的拓扑网络中速率高达 8 Mbps

4 Ordering Information

Part Number	Marking Code	Package Type	Shipping Qty
UMCAN1044VS8	1044VS8	SOP8	3000pcs/13Inch Tape & Reel
UMCAN1044VDA	1044V	DFN8 3.0×3.0	3000pcs/13Inch Tape & Reel
UMCAN1044NS8	1044NS8	SOP8	3000pcs/13Inch Tape & Reel
UMCAN1044NDA	1044N	DFN8 3.0×3.0	3000pcs/13Inch Tape & Reel

5 Pin Configuration and Function

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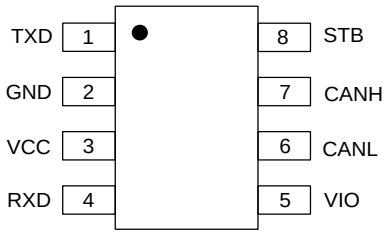
<td> 
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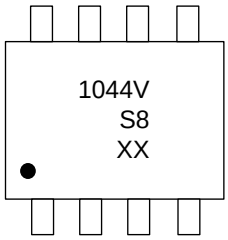
<td> 

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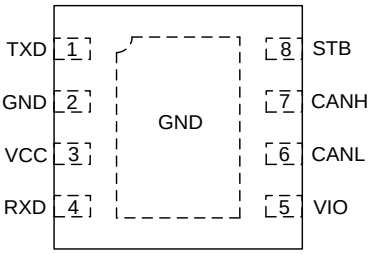
<td> 
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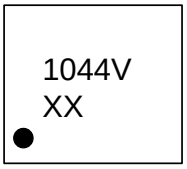
<td> 

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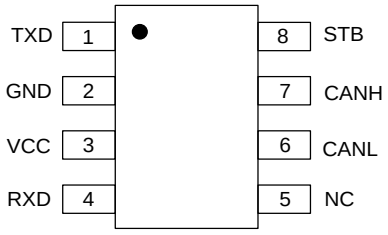
<td> 
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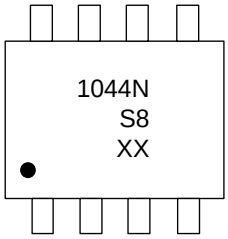
<td> 

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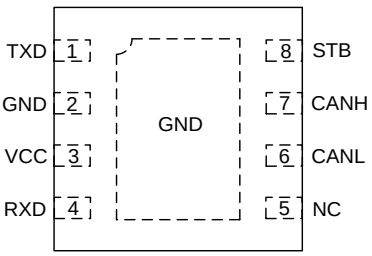
<td> 
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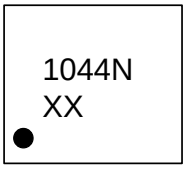
<td> 

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5 Pin Configuration and Function (continued)

Table 5-1. Pin Functions

Pin No.	Symbol	Description
1	TXD	Transmit data input
2	GND	Ground (Note 1)
3	V_{CC}	Supply voltage
4	RXD	Receive data output; reads out data from the bus lines
5	NC	Not connected in UMCAN1044NS8 and UMCAN1044NDA versions
	V_{IO}	Supply voltage for I/O level adapter
6	CANL	Low-level CAN bus line
7	CANH	High-level CAN bus line
8	STB	Standby mode control input

Note 1: DFN8 package die supply ground is connected to both the GND pin and the exposed center pad. The GND pin must be soldered to board ground. For enhanced thermal and electrical performance, it is recommended that the exposed center pad also be soldered to board ground.

6 Specifications

6.1 Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Bus supply voltage		4.5		5.5	V
V_{IO}	Supply voltage I/O level shifter		2.9		5.5	V
T_A	Operating ambient temperature		-40		125	℃

6.2 Absolute Maximum Ratings (Note 1, 2, 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Bus supply voltage		-0.3		+7	V
V_{IO}	Supply voltage I/O level shifter		-0.3		+7	V
V_{BUS}	Voltage range on CANH, CANL		-40		+40	V
V_{DIF}	Voltage range between CANH and CANL		-40		+40	V
V_I	Voltage range on STB	Note 4	-0.3		V_{IO}+0.3	V
	Voltage range on TXD	Note 4	-0.3		V_{IO}+0.3	V
V_O	Voltage range on RXD	Note 4	-0.3		V_{IO}+0.3	V
V_{trt}	Transient voltage on CANH, CANL pins (Note 5)	pulse 1	-100			V
		pulse 2a			+75	V
		pulse 3a	-150			V
		pulse 3b			+100	V
V_{ESD}	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	All pins		±8		kV
	Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002	All pins		±2		kV
	Contact discharge, per IEC 61000-4-2	Bus pins		±10		kV
I_{LU}	Latch up, per JEDEC JESD78	Class II		800		mA
T_{VJ}	Virtual junction temperature		-40		150	℃
T_{STG}	Storage temperature		-55		150	℃

Note 1: Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
Note 2: All voltage values, except differential I/O bus voltages, are with respect to ground terminal.
Note 3: $V_{IO} = V_{CC}$ in non-VIO product variants.
Note 4: Maximum voltage should never exceed 7 V.
Note 5: Verified by an external test house according to IEC TS 62228, Section 4.2.4; parameters for standard pulses defined in ISO 7637.

6.3 Electrical Characteristics (Static) (Note 1)

T_J = -40℃ to +150℃; V_{CC} = 4.5V to 5.5V; V_{IO} = 2.9V to 5.5V (Note1); R_L = 60Ω; C_L = 100pF unless otherwise specified; All voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply；pin VCC						
$V_{UVD(STB)}$	Standby undervoltage detection voltage on pin VCC		3.5	4	4.3	V
$V_{UVD(SWOFF)VCC}$	Switch-off undervoltage detection voltage on pin VCC	Variants without V_{IO}	2.4	2.6	2.8	V
I_{CC}	Supply current	Variants without a V_{IO} pin; STB = V_{CC}; TXD = V_{CC}		10	17.5	uA
		Variants with a VIO pin; STB = V_{IO}; TXD = V_{IO}		0.1	1	uA
		STB = 0 V; TXD = V_{IO}		1.6	5	mA
		STB = 0 V; TXD = 0	20	45	60	mA
		STB = 0 V; TXD = 0 V; short circuit on bus lines; -3V < (CANH=CANL) < 18V		80	110	mA
I/O level adapter supply；pin VIO						
$V_{UVD(SWOFF)VIO}$	Switch-off undervoltage detection voltage on pin VIO	Variants with a VIO pin	2.4	2.6	2.8	V
I_{IO}	supply current on pin VIO	STB = V_{IO}; TXD = V_{IO}		8	16.5	uA
		STB = 0 V; TXD = V_{IO}	5	10	30	uA
		STB = 0 V; TXD = 0V		110	300	uA
Standby mode control input; pin STB						
V_{IH}	High-level input voltage		0.7V_{IO}			V
V_{IL}	Low-level input voltage				0.3V_{IO}	V
I_{IH}	High-level input current	STB = V_{IO}	-1		1	uA
I_{IL}	Low-level input current	STB = 0 V	-15		-1	uA

6.3 Electrical Characteristics (Static)---continued (Note 1)

T_J = -40℃ to +150℃; V_{CC} = 4.5V to 5.5V; V_{IO} = 2.9V to 5.5V; R_L = 60Ω; C_L = 100pF unless otherwise specified; All voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CAN transmit data input; pin TXD						
V_{IH}	High-level input voltage		$0.7V_{IO}$			V
V_{IL}	Low-level input voltage				$0.3V_{IO}$	V
I_{IH}	High-level input current	TXD = V_{IO}	-5		5	uA
I_{IL}	Low-level input current	TXD = 0 V	-270	-100	-60	uA
C_I	Input capacitance			5	10	pF
CAN receive data output; pin RXD						
I_{OH}	High-level output current	RXD = V_{IO} - 0.4 V	-9	-1.5		mA
I_{OL}	Low-level output current	RXD = 0.4V		1.5	12	mA
Driver						
$V_{O(DOM)}$	Dominant output voltage	STB = 0 V; TXD = 0 V; $t < t_{TO(DOM)TXD}$; 50 Ω ≤ R_L ≤ 65 Ω; pin CANH	2.75	3.5	4.5	V
		STB = 0 V; TXD = 0 V; $t < t_{TO(DOM)TXD}$; 50 Ω ≤ R_L ≤ 65 Ω; pin CANL	0.5	1.5	2.25	V
$V_{OD(DOM)}$	Dominant differential output voltage	STB = 0 V; TXD = 0 V; $t < t_{TO(DOM)TXD}$; 50 Ω ≤ R_L ≤ 65 Ω	1.5		3	V
		STB = 0 V; TXD = 0 V; $t < t_{TO(DOM)TXD}$; 45 Ω ≤ R_L ≤ 70 Ω	1.4		3.3	V
		STB = 0 V; TXD = 0 V; $t < t_{TO(DOM)TXD}$; R_L = 2240 Ω	1.5		5	V

6.3 Electrical Characteristics (Static)---continued (Note 1)

T_J = -40℃ to +150℃; V_{CC} = 4.5V to 5.5V; V_{IO} = 2.9V to 5.5V; R_L = 60Ω; C_L = 100pF unless otherwise specified; All voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{SYM(DOM)}$	Dominant output voltage symmetry, V_{CC} - CANH – CANL	STB = 0 V; TXD = 0 V; $t < t_{TO(DOM)TXD}$; R_L = 60 Ω	-400		400	mV
$V_{O(REC)}$	Recessive output voltage	STB = 0 V; TXD = V_{IO}; R_L = open	2	0.5V_{CC}	3	V
$V_{OD(REC)}$	Recessive differential output voltage	STB = 0 V; TXD = V_{IO}; R_L = open	-50		50	mV
$V_{O(STB)}$	Bus output voltage, Standby Mode	STB = V_{IO}; TXD = V_{IO}; R_L = open	-100		100	mV
$V_{OD(STB)}$	Bus differential output voltage, Standby Mode	STB = V_{IO}; TXD = V_{IO}; R_L = open	-200		200	mV
$V_{SYM(TX)}$	Transmitter output voltage symmetry, (CANH + CANL)/V_{CC}	STB = 0 V; TXD = 250 kHz, 1 MHz, 2.5MHz; R_L = 60 Ω; C_{SPLIT} = 4.7 nF	0.9V_{CC}		1.1V_{CC}	V
$I_{OS(DOM)}$	Dominant short-circuit output current	STB = 0 V; TXD = 0 V; VCC = 5 V; CANH = -15 V to 40 V; CANL = open	-100	-70		mA
		STB = 0 V; TXD = 0 V VCC = 5 V; CANL = -15 V to 40 V; CANH = open		70	100	mA
$I_{OS(REC)}$	Recessive short-circuit output current	STB = 0 V; TXD = V_{IO}; -27 V ≤ CANH = CANL ≤ 32 V	-5		5	mA
Receiver						
V_{TH}	Differential receiver threshold voltage, Normal mode	STB = 0 V; -15 V ≤ CANH, CANL ≤ 15 V	0.5		0.9	V
$V_{ID(DOM)}$	Receiver dominant voltage, Normal mode	STB = 0 V; -15 V ≤ CANH, CANL ≤ 15 V	0.9		9	V
$V_{ID(REC)}$	Receiver recessive voltage, Normal mode	STB = 0 V; -15 V ≤ CANH, CANL ≤ 15 V	-4		0.5	V
V_{HYS}	Differential receiver hysteresis voltage, Normal mode	STB = 0 V; -15 V ≤ CANH, CANL ≤ 15 V	50		300	mV

6.3 Electrical Characteristics (Static)---continued (Note 1)

T_J = -40℃ to +150℃; V_{CC} = 4.5V to 5.5V; V_{IO} = 2.9V to 5.5V; R_L = 60Ω; C_L = 100pF unless otherwise specified; All voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{TH(STB)}$	Differential receiver threshold voltage, Standby mode	STB = V_{IO}; -15 V ≤ CANH, CANL ≤ 15 V	0.4		1.15	V
$V_{ID(DOM)STB}$	Receiver dominant voltage, Standby mode	STB = V_{IO}; -15 V ≤ CANH, CANL ≤ 15 V	1.15		9	V
$V_{ID(REC)STB}$	Receiver recessive voltage, Standby	STB = V_{IO}; -15 V ≤ CANH, CANL ≤ 15 V	-4		0.4	V
$I_{LKG(PD)}$	Unpowered Leakage current	V_{CC} = V_{IO} = 0 V or shorted to GND via 47 kΩ; CANH = CANL = 5 V	-5		18	uA
R_I	Input resistance	STB = 0 V; TXD = V_{IO}; -2 V ≤ CANH, CANL ≤ 7 V	15	30	40	kΩ
ΔR_I	Input resistance deviation, [1 − ($R_{IN(CANH)}$ / $R_{IN(CANL)}$)] × 100 %	STB = 0 V; TXD = V_{IO}; -2 V ≤ CANH, CANL ≤ 7 V	-3		3	%
R_{ID}	Differential input resistance	STB = 0 V; TXD = V_{IO}; -2 V ≤ CANH, CANL ≤ 7 V	30	60	80	kΩ
C_{IN}	Common-mode input capacitance to ground				20	pF
C_{ID}	Differential input capacitance				10	pF
Thermal Protection						
$T_{J(SD)}$	Thermal shutdown threshold	Temperature rising		185		℃

Note 1: V_{IO} = V_{CC} in non-VIO product variants.

6.4 Electrical Characteristics (Dynamic) (Note 1)

T_J = -40℃ to +150℃; V_{CC} = 4.5V to 5.5V; V_{IO} = 2.9V to 5.5V; R_L = 60Ω; C_L = 100pF unless otherwise specified; all voltages are defined with respect to ground.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Transceiver timing; pins CANH, CANL, TXD and RXD; See figure 7-1 and figure 7-3						
$t_{D(TXD-BUSDOM)}$	Delay time from TXD to bus dominant	STB = 0 V		58	90	ns
$t_{D(TXD-BUSREC)}$	Delay time from TXD to bus recessive	STB = 0 V		58	90	ns
$t_{D(BUSDOM -RXD)}$	Delay time from bus dominant to RXD	STB = 0 V		60	115	ns
$t_{D(BUSREC -RXD)}$	Delay time from bus recessive to RXD	STB = 0 V		60	110	ns
$t_{D(TXDL-RXDL)}$	Delay time from TXD LOW to RXD LOW	STB = 0 V	50		255	ns
$t_{D(TXDH-RXDH)}$	Delay time from TXD HIGH to RXD HIGH	STB = 0 V	50		255	ns
CAN FD timing characteristics according to ISO 11898-2:2024 parameter set B ($t_{BIT(TXD)}$) ⩾ 200 ns, up to 5 Mbit/s); See figure 7-1 and figure 7-3						
$\Delta t_{BIT(BUS)}$	Transmitted recessive bit width deviation	$\Delta t_{BIT(BUS)}= t_{BIT(BUS)}- t_{BIT(TXD)}$	-45		10	ns
Δt_{REC}	Receiver timing symmetry	$\Delta t_{REC}= t_{BIT(RXD)}- t_{BIT(BUS)}$	-45		15	ns
$\Delta t_{BIT(RXD)}$	Received recessive bit width deviation	$\Delta t_{REC}= t_{BIT(RXD)}- t_{BIT(TXD)}$	-80		20	ns
CAN FD timing characteristics according to ISO 11898-2:2024 parameter set A ($t_{BIT(TXD)}$) ⩾ 500 ns, up to 2 Mbit/s); See figure 7-1 and figure 7-3						
$\Delta t_{BIT(BUS)}$	Transmitted recessive bit width deviation	$\Delta t_{BIT(BUS)}= t_{BIT(BUS)}- t_{BIT(TXD)}$	-65		30	ns
Δt_{REC}	Receiver timing symmetry	$\Delta t_{REC}= t_{BIT(RXD)}- t_{BIT(BUS)}$	-65		40	ns
$\Delta t_{BIT(RXD)}$	Received recessive bit width deviation	$\Delta t_{REC}= t_{BIT(RXD)}- t_{BIT(TXD)}$	-100		50	ns
Dominant time-out time						
$t_{TO(DOM)TXD}$	TXD dominant time-out time	STB = 0 V; TXD = 0V, (Note 2)	0.8	2.6	6.5	ms
Mode transitions						
$t_{D(STB-NRM)}$	Mode change time, from standby to normal	(Note 3)	7	15	47	us

6.4 Electrical Characteristics (Dynamic) --- continued (Note 1)

T_J = -40℃ to +150℃; V_{CC} = 4.5V to 5.5V; V_{IO} = 2.9V to 5.5V; R_L = 60Ω; C_L = 100pF unless otherwise specified; all voltages are defined with respect to ground.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Bus wake-up timing; pins CANH and CANL; See figure 9-1						
$t_{WK(BUSDOM)}$	Bus dominant wake-up time	STB = V_{IO}, (Note 4)	0.5		1.8	us
$t_{WK(BUSREC)}$	Bus recessive wake-up time	STB = V_{IO}, (Note 4)	0.5		1.8	us
$t_{TO(WK)BUS}$	Bus wake-up time-out time	STB = V_{IO}, (Note 2)	0.8	3.5	6.5	ms
$t_{FLTR(WK)BUS}$	Bus wake-up filter time	STB = V_{IO}, (Note 5)	0.5		1.8	us

Note 1: V_{IO} = V_{CC} in non-VIO product variants.
Note 2: Time-out occurs between the min and max values. Time-out is guaranteed not to occur below the min value; time-out is guaranteed to occur above the max value.
Note 3: Standby-to-Normal mode transition occurs between the min and max values. It is guaranteed not to occur below the min value; it is guaranteed to occur above the max value.
Note 4: A dominant/recessive phase shorter than the min value is guaranteed not be seen as a dominant/recessive bit; a dominant/recessive phase longer than the max value is guaranteed to be seen as a dominant/recessive bit.
Note 5: Pulses shorter than the min value are guaranteed to be filtered out; pulses longer than the max value are guaranteed to be processed.

7 Parameter Measurement Information

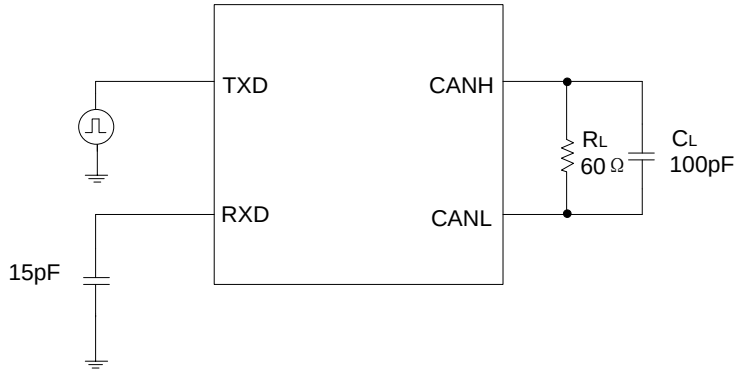


Figure 7-1. CAN transceiver timing test circuit

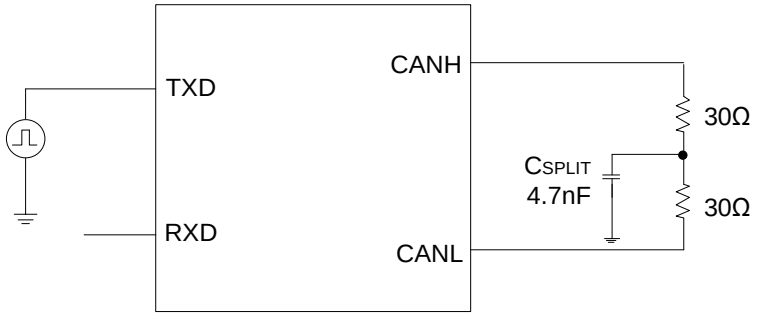


Figure 7-2. Test circuit for measuring transceiver transmitter driver symmetry

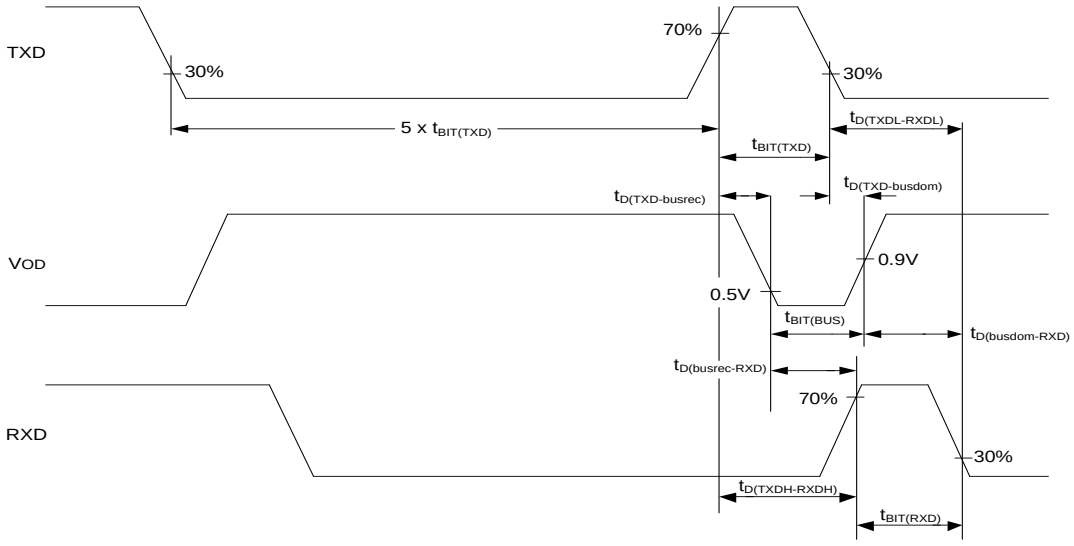
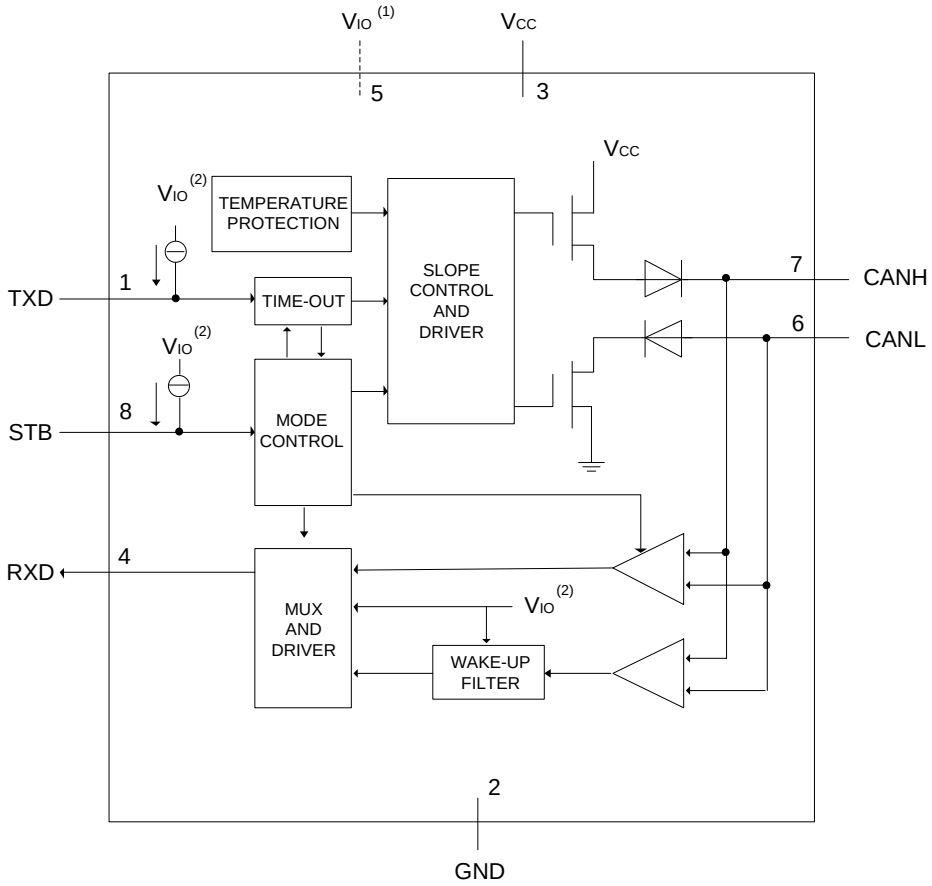


Figure 7-3. CAN FD timing definitions according to ISO 11898-2:2024

8 Block diagram



Note1: Pin 5 is not connected in non-VIO product variants.
Note2: V_{IO} = V_{CC} in non-VIO product variants.

Figure 8-1. Block diagram

9 Detailed Description

9.1 Operating modes

The UMCAN1044 supports three operating modes, Normal Standby. The operating mode is selected via pin STB. See Table for a description of the operating modes under normal supply conditions.

Mode	Inputs		Outputs	
	Pin STB	Pin TXD	CAN driver	Pin RXD
Normal	LOW	LOW	dominant	LOW
		HIGH	recessive	LOW when bus dominant
				HIGH when bus recessive
Standby	HIGH	x (Note1)	biased to ground	follows BUS when wake-up detected
				HIGH when no wake-up detected
Off	x	x	Hi-Z state	Hi-Z state

Note1: 'x' = don't care.

9.1.1 Normal mode

A LOW level on pin STB selects Normal mode. In this mode, the transceiver can transmit and receive data via the bus lines CANH and CANL (see Figure 8-1 for the block diagram). The differential receiver converts the analog data on the bus lines into digital data which is output on pin RXD. The slopes of the output signals on the bus lines are controlled internally.

9.1.2 Standby mode

A HIGH level on pin STB selects Standby mode. In Standby mode, the transceiver is not able to transmit or correctly receive data via the bus lines. The transmitter and Normal mode receiver blocks are switched off to reduce supply current, and only a low-power differential receiver monitors the bus lines for activity.
In Standby mode, the bus lines are biased to ground to minimize system supply current. The low-power receiver is supplied from V_{IO} (V_{CC} in non-V_{IO} variants) and can detect CAN bus activity even if V_{IO} is the only available supply voltage. Pin RXD follows the bus after a wake-up request has been detected. A transition to Normal mode is triggered when STB is forced LOW.

9.2 Remote wake-up (via the CAN bus)

The UMCAN1044 wakes up from Standby mode when a dedicated wake-up pattern (specified in ISO 11898-2:2024) is detected on the bus. This filtering helps avoid spurious wake-up events. A spurious wake-up sequence could be triggered by, for example, a dominant clamped bus or by dominant phases due to noise or spikes on the bus.
The wake-up pattern consists of:

- a dominant phase of at least $t_{WK(BUSDOM)}$ followed by
- a recessive phase of at least $t_{WK(BUSREC)}$ followed by
- a dominant phase of at least $t_{WK(BUSDOM)}$

9.2 Remote wake-up (via the CAN bus)---continued

Dominant or recessive bits between the above mentioned phases that are shorter than $t_{WK(BUSDOM)}$ and $t_{WK(BUSREC)}$ respectively are ignored.
The complete dominant-recessive-dominant pattern must be received within $t_{TO(WK)BUS}$ to be recognized as a valid wake-up pattern. Otherwise, the internal wake-up logic is reset. The complete wake-up pattern will then need to be retransmitted to trigger a wake-up event. Pin RXD remains HIGH until the wake-up event has been triggered.
After a wake-up sequence has been detected, the UMCAN1044 will remain in Standby mode with the bus signals reflected on RXD. Note that dominant or recessive phases lasting less than $t_{FLTR(WK)BUS}$ will not be detected by the low-power differential receiver and will not be reflected on RXD in Standby mode.
A wake-up event is not flagged on RXD if any of the following events occurs while a valid wake-up pattern is being received:

- The UMCAN1044 switches to Normal mode
- The complete wake-up pattern was not received within $t_{TO(WK)BUS}$
- A V_{CC} or V_{IO} undervoltage is detected (V_{CC} < $V_{UVD(SWOFF)VCC}$ or V_{IO} < $V_{UVD(SWOFF)VIO}$; see 9.3.3)

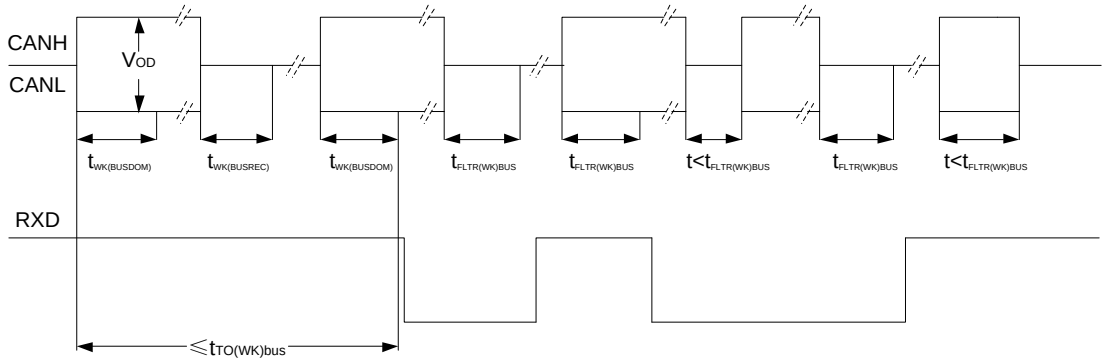


Figure 9-1. Wake-up Timing

9.3 Fail-safe features

9.3.1 TXD dominant time-out function

A 'TXD dominant time-out' timer is started when pin TXD is set LOW. If the LOW state on this pin persists for longer than $t_{TO(DOM)TXD}$, the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when pin TXD is set HIGH.

9.3.2 Internal biasing of TXD and STB input pins

Pins TXD and STB have internal pull-ups to V_{CC} (V_{IO} for variants with a V_{IO} pin) to ensure a safe, defined state in case one or both of these pins are left floating. Pull-up currents flow in these pins in all states; both pins should be held HIGH in Standby mode to minimize supply current.

9.3.3 Undervoltage detection on pins V_{CC} and V_{IO}

If V_{CC} drops below the standby undervoltage detection level, $V_{UVD(STB)VCC}$, the transceiver switches to Standby mode. The logic state of pin STB is ignored until V_{CC} has recovered.
In versions with a V_{IO} pin, if V_{IO} drops below the switch-off undervoltage detection level ($V_{UVD(SWOFF)VIO}$), the transceiver switches off and disengages from the bus (zero load) until V_{IO} has recovered.
In versions without a V_{IO} pin, if V_{CC} drops below the switch-off undervoltage detection level ($V_{UVD(SWOFF)VCC}$), the transceiver switches off and disengages from the bus (zero load) until V_{CC} has recovered.

9.3.4 Overtemperature protection

The output drivers are protected against overtemperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature, $T_{J(SD)}$, both output drivers are disabled. When the virtual junction temperature drops below $T_{J(SD)}$ again, the output drivers recover once TXD has been reset to HIGH. Including the TXD condition prevents output driver oscillation due to small variations in temperature.

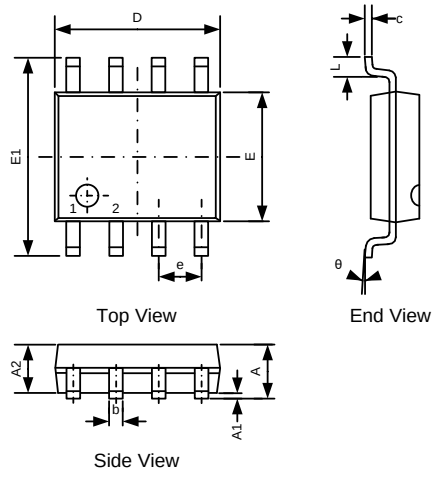
9.3.5 V_{IO} supply pin

Pin V_{IO} should be connected to the microcontroller supply voltage. This will adjust the signal levels of pins TXD, RXD and STB to the I/O levels of the microcontroller. Pin V_{IO} also provides the internal supply voltage for the low-power differential receiver in the transceiver. For applications running in low-power mode, this allows the bus lines to be monitored for activity even if there is no supply voltage on pin V_{CC}.
For variants of the UMCAN1044 without a V_{IO} pin, all circuitry is connected to V_{CC} (pin 5 is not bonded). The signal levels of pins TXD, RXD and STB are then compatible with 5 V microcontrollers. This allows the device to interface with both 3.3 V and 5 V-supplied microcontrollers, provided the microcontroller I/Os are 5 V tolerant.

10 Package Information

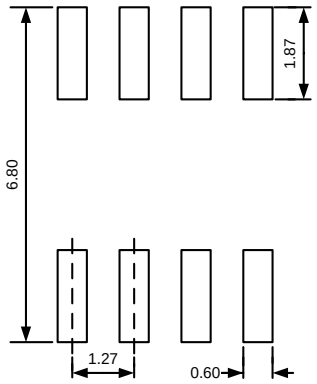
SOP8

Outline Drawing



Symbol	DIMENSIONS					
	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	1.35	1.55	1.75	0.053	0.061	0.069
A1	0.10	–	0.25	0.004	–	0.010
A2	1.25	–	1.65	0.049	–	0.065
b	0.30	–	0.51	0.012	–	0.020
c	0.15	–	0.25	0.006	–	0.010
D	4.70	4.90	5.10	0.185	0.193	0.200
E	3.80	3.90	4.00	0.150	0.154	0.157
E1	5.80	6.00	6.20	0.228	0.236	0.244
e	1.27BSC			0.050 BSC		
L	0.40	–	1.27	0.015	–	0.050
θ	0 °	–	8 °	0 °	–	8 °

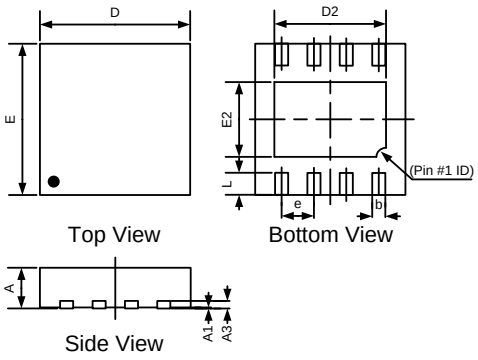
Land Pattern



NOTES:
1. Compound dimension: 4.90×3.90;
2. Unit: mm;
3. General tolerance ±0.05mm unless otherwise specified;
4. The layout is just for reference.

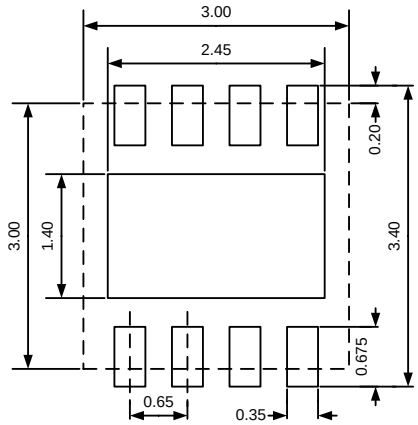
DFN8 3.0×3.0

Outline Drawing



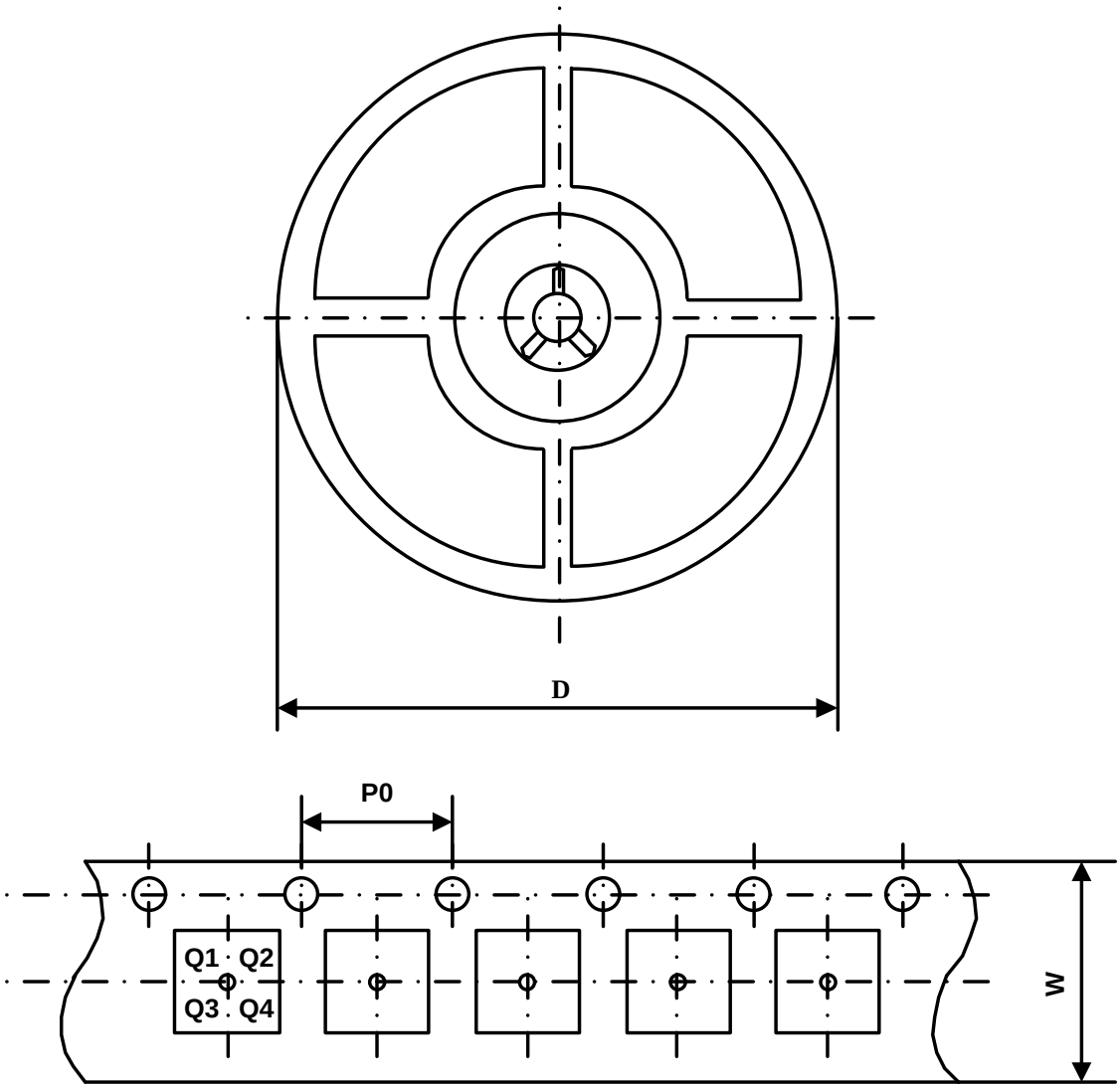
DIMENSIONS						
Symbol	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	0.57	-	0.80	0.022	-	0.031
A1	0.00	-	0.05	0.000	-	0.002
A3	0.20REF			0.008REF		
b	0.20	-	0.35	0.008	-	0.014
D	2.90	3.00	3.10	0.114	0.118	0.122
D2	2.15	-	2.55	0.085	-	0.100
E	2.90	3.00	3.10	0.114	0.118	0.122
E2	1.40	-	1.75	0.055	-	0.069
e	0.65BSC			0.026BSC		
L	0.30	-	0.60	0.012	-	0.024

Land Pattern



NOTES:
1. Compound dimension: 3.00×3.00;
2. Unit: mm;
3. General tolerance ±0.05mm unless otherwise specified;
4. The layout is just for reference.

Packing Information



Part Number	Package Type	Carrier Width (W)	Pitch (P0)	Reel Size (D)	PIN 1 Quadrant
UMCAN1044VS8	SOP8	12 mm	4 mm	330 mm	Q1
UMCAN1044VDA	DFN8 3.0×3.0	12 mm	4 mm	330 mm	Q1
UMCAN1044NS8	SOP8	12 mm	4 mm	330 mm	Q1
UMCAN1044NDA	DFN8 3.0×3.0	12 mm	4 mm	330 mm	Q1

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http://www.union–ic.com/index.aspx?cat_code=RoHSDeclaration

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