

用于彩色LCD接口的8路ESD/EMI保护 UM8411Z DFN16 3.3×1.3

描述

UM8411Z是一款集成TVS二极管的低通滤波器阵列。该器件专为抑制便携式电子设备中不需要的EMI/RFI信号并提供静电放电 (ESD) 保护而设计。这款先进的器件采用硅雪崩技术,具有卓越的钳位性能和直流电气特性。经过优化,可保护手机及其他便携式电子设备中的LCD。

该器件由8路相同的电路组成,每路都集成了用于ESD保护的TVS二极管和EMI/RFI滤波的RC网络。该器件集成了100Ω的串联电阻和10pF的电容,可在800MHz至2.5GHz范围内实现25dB的最小衰减。TVS二极管可有效抑制超过±15kV(空气间隙放电)和±8kV(接触放电)的ESD电压,符合IEC 61000-4-2标准的第4级要求。

UM8411Z 采用符合RoHS规范的16引脚 DFN16封装。尺寸为3.3 mm×1.3 mm。引脚间距为 0.4mm,表面采用无铅镍钯处理。该小型封装使其非常适合用于手机、数码相机和PDA等便 携式电子产品。

应用

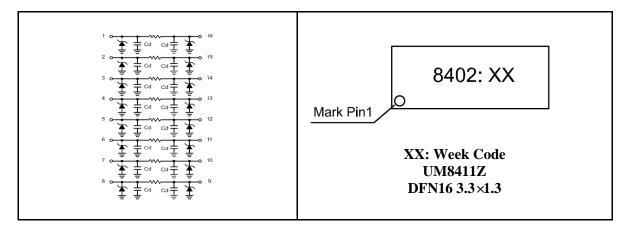
- 数据线的EMI滤波和ESD保护
- 无线电话
- 手持设备
- 笔记本电脑
- LCD 显示

特性

- 集成 TVS 的 EMI/RFI 滤波器,提供静电放电(ESD)保护
- ESD 保护符 IEC 61000-4-2 第 4 级要求: ±15kV (空气间隙放电) ±8kV (接触放电)
- 25dB 最小衰减: 800MHz 至 2.5GHz
- 工作电压: 5V
- 串联电阻: 100Ω±15%
- 典型电容: 10pF(V_R=2.5V)
- 固态硅雪崩技术
- DFN16 封装: 3.3mm×1.3 mm
- 湿度敏感等级: 1级

引脚配置

顶部视图





Ordering Information

Part Number	Working Voltage	Packaging Type	Channel	Marking Code	Shipping Qty
UM8411Z	5.0V	DFN16 3.3×1.3	8	8402	3000pcs/7 Inch Tape & Reel Tape Size: 12mm

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Junction Temperature	T_{J}	125	$\mathcal C$
Steady State Power per Resistor @ 25 °C	P_R	328	mW
Operating Temperature Range	T_{OP}	-40 to 85	$\mathcal C$
Storage Temperature Range	T_{STG}	-55 to 150	$\mathcal C$
Maximum Lead Temperature for Soldering	$T_{ m L}$	260	${\mathbb C}$

Electrical Characteristics

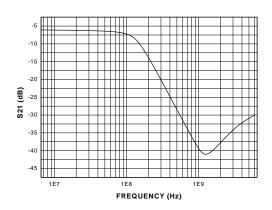
Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit
Reverse Stand-Off Voltage	V_{RWM}				5.0	V
Reverse Breakdown Voltage	V_{BR}	I _T =1mA	6.0	7.0	8.0	V
Reverse Leakage Current	I_R	$V_{RWM}=3.3V$			100	nA
Total Series Resistance	R_A	I _R =20mA, Each Line	85	100	115	Ω
Total Capacitance	C_{d}	Input to GND, Each Line $V_R=0V$, $f=1MHz$	16	20	24	pF
Total Capacitance	C_{d}	Input to GND, Each Line V _R =2.5V, f=1MHz	9	10	12	pF
Cut-Off Frequency (Note 1)	$ m f_{3dB}$	Above this frequency, appreciable attenuation occurs		150		MHz

Note 1: 50Ω source and 50Ω load termination.

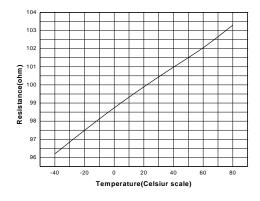


Typical Operating Characteristics

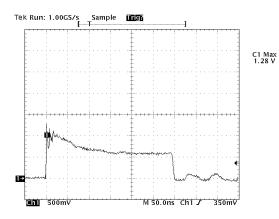
Typical Insertion Loss S21



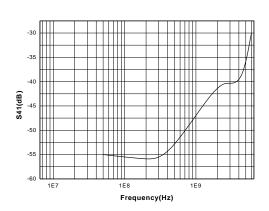
Typical Resistance vs. Temperature



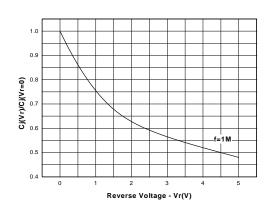
ESD Clamping (+8kV Contact)



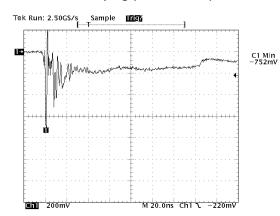
Analog Crosstalk Curve (S41)



Capacitance vs. Reverse Voltage



ESD Clamping (-8kV Contact)





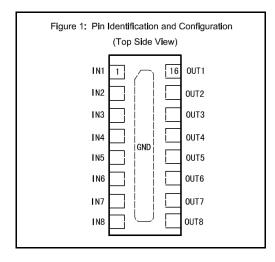
Applications Information

Device Connection

The UM8411Z is comprised of eight identical circuits each consisting of a low pass filter for EMI/RFI suppression and dual TVS diodes for ESD protection. The device is in a 16-pin DFN package. Electrical connection is made to the 16 pins located at the bottom of the device. A center tab serves as the ground connection. The device has a flow through design for easy layout. All path lengths should be kept as short as possible to minimize the effects of parasitic inductance in the board traces. Recommendations for the ground connection are given below.

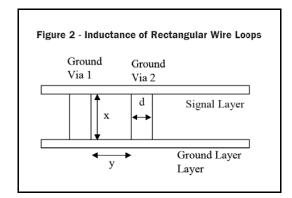
Ground Connection Recommendation

Parasitic inductance present in the board layout will affect the filtering performance of the device. As frequency increases, the effect of the inductance becomes more dominant. This effect is given by Equation 1.



Pin	Identification			
1 - 8	Input Lines			
7 - 16	Output Lines			
Center Tab	Ground			
Equation 1: The Impedance of an Inductor at Frequency XLF				
$XLF(L, f) = 2 \times_{\pi} \times f \times L$ Where: L= Inductance (H) f = Frequency (Hz)				

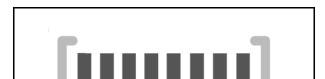
Via connections to the ground plane form rectangular wire loops or ground loop inductance as shown in Figure 2. Ground loop inductance can be reduced by using multiple vias to make the connection to the ground plane. Bringing the ground plane closer to the signal layer (preferably the next layer) also reduces ground loop inductance. Multiple vias in the device ground pad will result in a lower inductive ground loop over two exterior vias. Vias with a diameter d are separated by a distance y run between layers separated by a distance x. The inductance of the loop path is given by Equation 2. Thus, decreasing distance x and y will reduce the loop inductance and result in better high frequency filter characteristics.



Equation 2: Inductance of Rectangular Wire Loop $LRECT(d,x,y) = 10.16*10^{-9}*\left[x*ln\left[\frac{2^{e}y}{d}\right] + y*ln\left[\frac{2^{e}x}{d}\right]\right]$ Where: d = Diameter of the Wire (in) x = Length of Wire Loop (in) y = Breath of Wire Loop (in)



Figure 3 shows the recommended device layout. The ground pad vias have a diameter of 0.008 inches (0.20mm) while the two external vias have a diameter of 0.010 inches (0.250mm). The internal vias are spaced approximately evenly from the center of the pad. The designer may choose to use more vias with a smaller diameter (such as 0.005 inches or 0.125mm) since changing the diameter of the via will result in little change in inductance (i.e. the log function in Equation 2 in highly insensitive to parameter d).



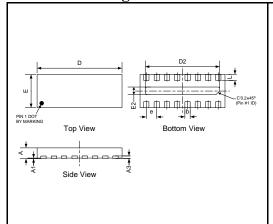
 $Figure \ 3-Recommended \ Layout \ Using \ Ground \ Vias$



Package Information

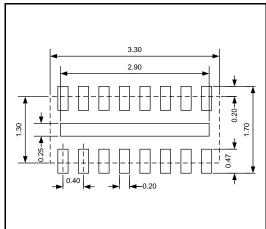
UM8411Z: DFN16 3.3×1.3

Outline Drawing



DIMENSIONS							
Symbol	MILLIMETERS			INCHES			
	Min	Тур	Max	Min	Typ	Max	
A	0.47	0.55	0.60	0.019	0.022	0.024	
A1	0.00	-	0.05	0.000	-	0.002	
A3	0.15REF		0.006REF				
b	0.15	0.20	0.25	0.006	0.008	0.010	
D	3.224	3.30	3.376	0.127	0.130	0.133	
D2	2.45	ı	3.00	0.096	1	0.118	
Е	1.25	1.30	1.426	0.049	0.051	0.056	
E2	0.20	-	0.50	0.008	-	0.020	
e	0.40TYP			0.016TYP			
L	0.17	-	0.37	0.007	-	0.015	

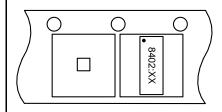
Land Pattern



NOTES:

- 1. Compound dimension: 3.30×1.30;
- 2. Unit: mm;
- 3. General tolerance ± 0.05 mm unless otherwise specified;
- 4. The layout is just for reference.

Tape and Reel Orientation





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