用于彩色LCD接口的8通道ESD-EMI防护

UM8401 *DFN16 4.0×1.6*

描述

UM8401 是一款集成TVS二极管的低通滤波器阵列。该器件专为抑制便携式电子设备中不需要的EMI/RFI信号并提供静电放电 (ESD) 保护而设计。这款先进的器件采用硅雪崩技术，具有卓越的钳位性能和直流电气特性。经过优化，可保护手机及其他便携式电子设备中的彩色液LCD。

UM8401 由 8 路相同的电路组成，每路都集成了用于ESD保护的TVS二极管和EMI/RFI滤波的RX网络。该器件集成了 100Ω的串联电阻和 10pF的电容，可在 800 MHz至 2.5GHz范围内实现 25dB 的最小衰减。TVS二极管可有效抑制超过 ±15kV（空气间隙放电）和 ±8kV（接触放电）的ESD电压，符合IEC 61000-4-2 标准的第 4 级要求。

UM8401 采用符合 RoHS 标准的 16 引脚 DFN16 4.0×1.6 封装。引脚间距为 0.5mm，表面采用无铅镍钯处理。该小型封装使其非常适合用于手机、数码相机和PDA等便携式电子产品。

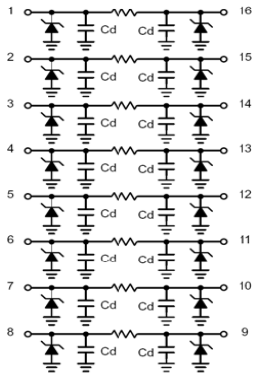
应用

- 数据线的EMI滤波和ESD保护
- 无线电话
- 手持式产品
- 笔记本电脑
- LCD显示器

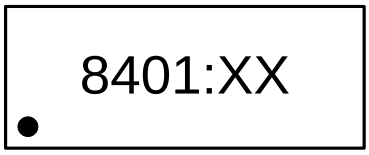
特性

- 集成 TVS 的 EMI/RFI 滤波器，提供静电放电（ESD）保护
- ESD 保护符合 IEC 61000-4-2 第 4 级要求：
  ±15kV（空气放电）
  ±8kV（接触放电）
- 25dB 最小衰减：800MHz 至 2.5GHz
- 工作电压：5V
- 电阻：100Ω ±15%
- 典型电容：15pF (V_R=2.5V)
- 固态硅雪崩技术
- DFN16 封装：4.0mm ×1.6 mm
- 湿度敏感等级：1 级

引脚配置



俯视图



XX: Week Code
UM8401
DFN16 4.0×1.6

Ordering Information

Part Number	Working Voltage	Packaging Type	Channel	Marking Code	Shipping Qty
UM8401	5.0V	DFN16 4.0×1.6	8	8401	3000pcs/7 Inch Tape & Reel

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Junction Temperature	T_J	125	℃
Steady State Power per Resistor @ 25℃	P_R	328	mW
Operating Temperature Range	T_{OP}	-40 to 85	℃
Storage Temperature Range	T_{STG}	-55 to 150	℃
Maximum Lead Temperature for Soldering	T_L	260	℃

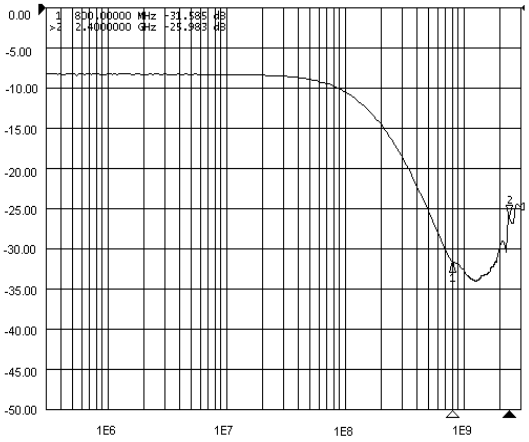
Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Reverse Stand-Off Voltage	V_{RWM}				5.0	V
Reverse Breakdown Voltage	V_{BR}	I_T=1mA	6.0	7.0	8.0	V
Reverse Leakage Current	I_R	V_{RWM}=3.3V			100	nA
Total Series Resistance	R_A	I_R=20mA, Each Line	85	100	115	Ω
Total Capacitance	C_d	Input to GND, Each Line V_R=0V, f=1MHz	20	23	26	pF
Total Capacitance	C_d	Input to GND, Each Line V_R=2.5V, f=1MHz	13	15	18	pF
Cut-Off Frequency (Note 1)	f_{3dB}	Above this frequency, appreciable attenuation occurs		150		MHz

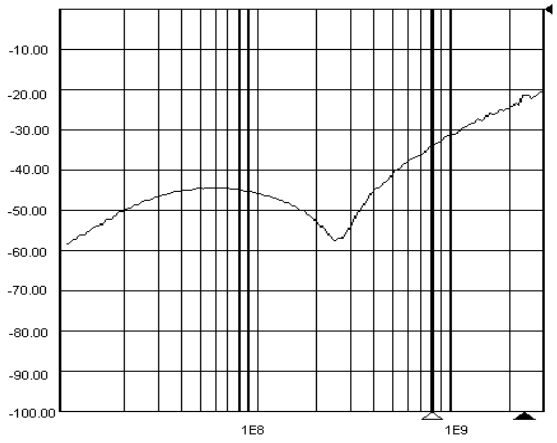
Note 1: 50Ω source and 50Ω load termination.

Typical Operating Characteristics

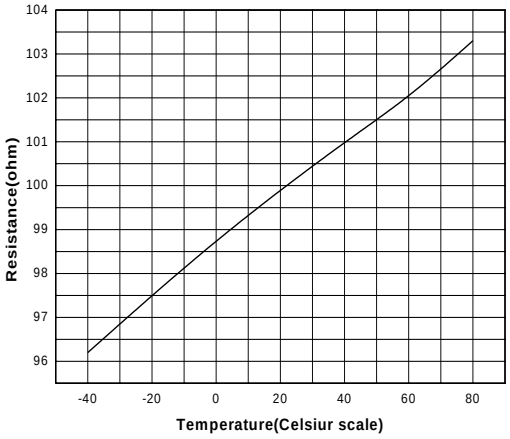
Typical Insertion Loss S21



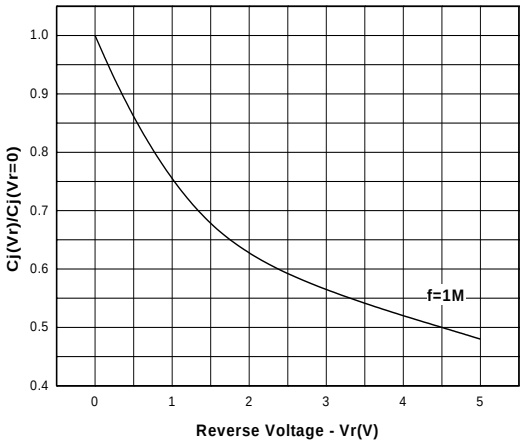
Analog Crosstalk Curve (S41)



Typical Resistance vs. Temperature



Capacitance vs. Reverse Voltage



Applications Information

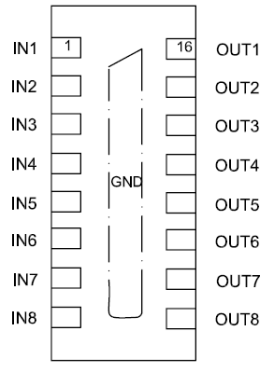
Device Connection

The UM8401 is comprised of eight identical circuits each consisting of a low pass filter for EMI/RFI suppression and dual TVS diodes for ESD protection. The device is in a 16-pin DFN package. Electrical connection is made to the 16 pins located at the bottom of the device. A center tab serves as the ground connection. The device has a flow through design for easy layout. All path lengths should be kept as short as possible to minimize the effects of parasitic inductance in the board traces. Recommendations for the ground connection are given below.

Ground Connection Recommendation

Parasitic inductance present in the board layout will affect the filtering performance of the device. As frequency increases, the effect of the inductance becomes more dominant. This effect is given by Equation 1.

Figure1: Pin Identificaton & Configuration
(Top Side View)



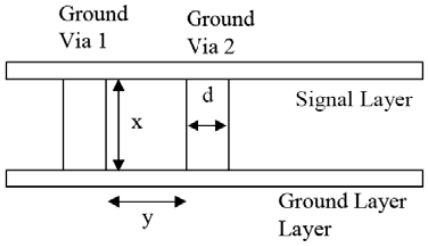
Pin	Identification
1 - 8	Input Lines
9 - 16	Output Lines
Center Tab	Ground

Equation 1: The Impedance of an Inductor at Frequency XLF

$XLF(L, f) = 2 \times \pi \times f \times L$
Where:
L= Inductance (H)
f = Frequency (Hz)

Via connections to the ground plane form rectangular wire loops or ground loop inductance as shown in Figure 2. Ground loop inductance can be reduced by using multiple vias to make the connection to the ground plane. Bringing the ground plane closer to the signal layer (preferably the next layer) also reduces ground loop inductance. Multiple vias in the device ground pad will result in a lower inductive ground loop over two exterior vias. Vias with a diameter d are separated by a distance y run between layers separated by a distance x. The inductance of the loop path is given by Equation 2. Thus, decreasing distance x and y will reduce the loop inductance and result in better high frequency filter characteristics.

Figure 2 - Inductance of Rectangular Wire Loops



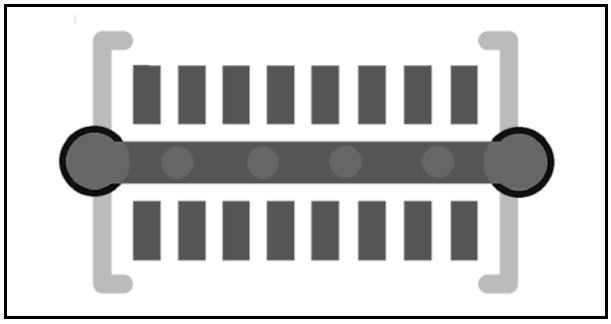
Equation 2: Inductance of Rectangular Wire Loop

$$LRECT(d, x, y) = 10.16 * 10^{-9} * \left[x * \ln\left[\frac{2*y}{d}\right] + y * \ln\left[\frac{2*x}{d}\right]\right]$$

Where:
d = Diameter of the wire (in)
x = Length of wire loop (in)
y = Breath of wire loop (in)

Figure 3 shows the recommended device layout. The ground pad vias have a diameter of 0.008 inches (0.20 mm) while the two external vias have a diameter of 0.010 inches (0.250mm). The internal vias are spaced approximately evenly from the center of the pad. The designer may choose to use more vias with a smaller diameter (such as 0.005 inches or 0.125mm) since changing the diameter of the via will result in little change in inductance (i.e. the log function in Equation 2 in highly insensitive to parameter d) .

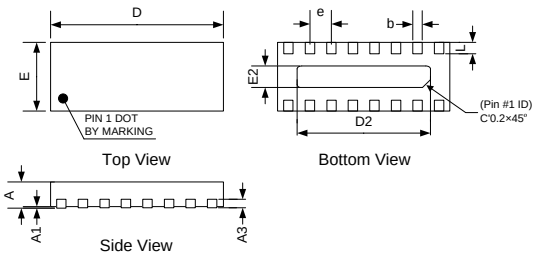
Figure 3 – Recommended Layout Using Ground Vias



Package Information

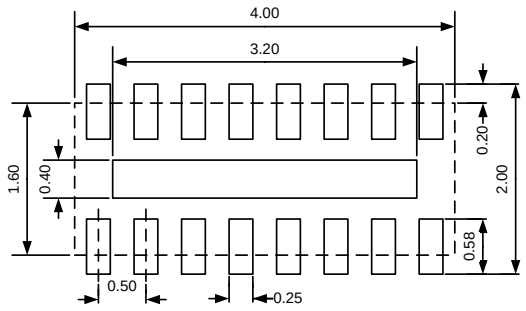
UM8401 DFN16 4.0×1.6

Outline Drawing



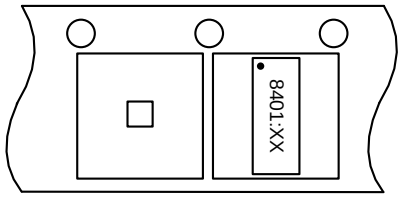
DIMENSIONS						
Symbol	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	0.50	-	0.80	0.020	-	0.031
A1	0.00	-	0.05	0.000	-	0.002
A3	0.203REF			0.008REF		
b	0.15	-	0.30	0.006	-	0.012
D	3.924	4.00	4.076	0.154	0.157	0.160
D2	2.95	-	3.30	0.116	-	0.130
E	1.524	1.60	1.676	0.060	0.063	0.066
E2	0.30	-	0.60	0.012	-	0.024
e	0.50TYP			0.020TYP		
L	0.15	-	0.38	0.006	-	0.015

Land Pattern



NOTES:
1. Compound dimension: 4.00×1.60;
2. Unit: mm;
3. General tolerance ±0.05mm unless otherwise specified;
4. The layout is just for reference.

Tape and Reel Orientation



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