

用于彩色 LCD 接口的6通道ESD/EMI保护

UM6411 DFN12 2.5×1.3

描述

UM6411是一款集成TVS二极管的低通滤波器阵列。该器件专为抑制便携式电子设备中不需要的EMI/RFI信号并提供静电放电 (ESD) 保护而设计。这款先进的器件采用固态硅雪崩技术，具有卓越的箝位性能和直流电气特性。其设计专门针对手机及其他便携式电子设备中的LCD提供保护。

UM6411由六路相同的电路组成，每路都集成了ESD保护的 TVS 二极管和用于 EMI/RFI 滤波的RX网络。该器件采用 100Ω 的串联电阻和 10pF 的电容，可在800MHz至2.5GHz范围内实现30dB的最小衰减。TVS二极管可有效抑制超过 $\pm 15\text{kV}$ （空气间隙放电）和 $\pm 8\text{kV}$ （接触放电）的ESD电压，符合IEC 61000-4-2标准的第4级要求。

UM6411 采用符合 RoHS 规范的12引脚DFN12 2.5mm×1.3mm 封装。引脚间距为 0.4mm，表面采用无铅镍钎处理。该小型封装使其非常适合用于手机、数码相机和 PDA 等便携式电子产品。

应用

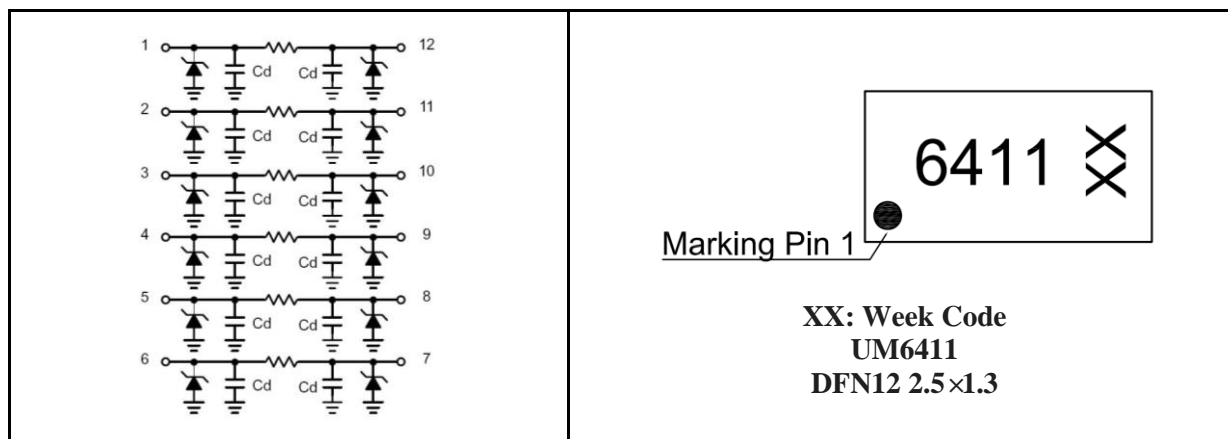
- 彩色液晶屏保护
- 手机 CCD 摄像头线路
- 手机底部连接器

特性

- 集成TVS保护的双向EMI/RFI滤波器
- ESD 保护符合 IEC 61000-4-2第4级要求：
 $\pm 15\text{kV}$ （空气间隙放电）， $\pm 8\text{kV}$ （接触放电）
- 30dB 最小衰减：800MHz 至 2.5GHz
- TVS工作电压：5V
- 电阻： $100\Omega \pm 15\%$
- 典型电容： 10pF ($V_R=2.5\text{V}$)
- 6通道ESD保护和滤波
- 固态硅雪崩技术

引脚配置

顶部视图



Ordering Information

Part Number	Working Voltage	Packaging Type	Channel	Marking Code	Shipping Qty
UM6411	5.0V	DFN12 2.5×1.3	6	6411	3000pcs/7 Inch Tape & Reel

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T _J	Junction Temperature	125	℃
P _R	Steady-State Power Per Resistor @ 25 ℃	328	mW
T _{OP}	Operating Temperature Range	-40 to 85	℃
T _{STG}	Storage Temperature Range	-55 to 150	℃
T _L	Maximum Lead Temperature for Soldering	260	℃

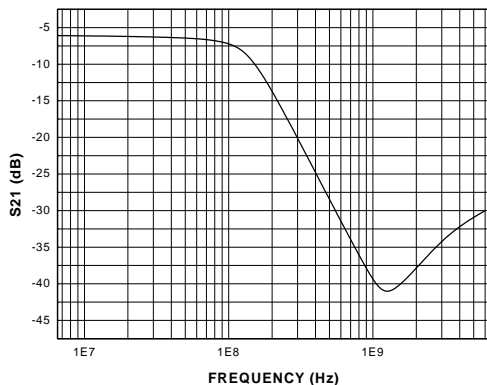
Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{RWM}	Reverse Stand-Off Voltage				5	V
V _{BR}	Reverse Breakdown Voltage	I _T =1mA	6	7	8	V
I _R	Reverse Leakage Current	V _{RWM} =3.0V			0.5	μA
R _A	Total Series Resistance	I _R =20mA Each Line	85	100	115	Ω
C _d	Total Capacitance	Input to GND, Each Line V _R =0V, f=1MHz	16	20	24	pF
C _d	Total Capacitance	Input to GND, Each Line V _R =2.5V, f=1MHz	9	10	12	pF
f _{3dB}	Cut-Off Frequency (Note 1)	Above this frequency, appreciable attenuation occurs		150		MHz

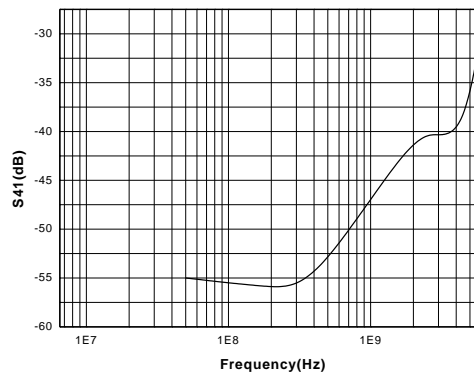
Note 1: 50Ω source and 50Ω load termination.

Typical Operating Characteristics

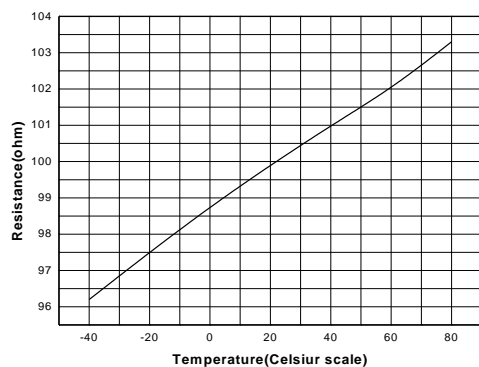
Typical Insertion Loss S21



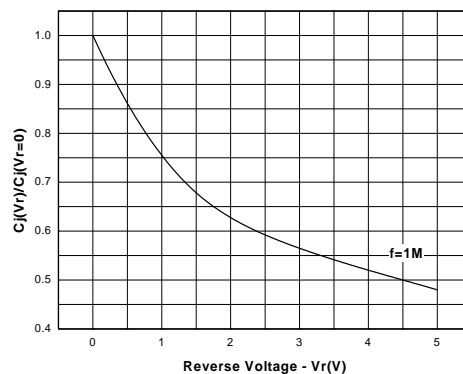
Analog Crosstalk Curve (S41)



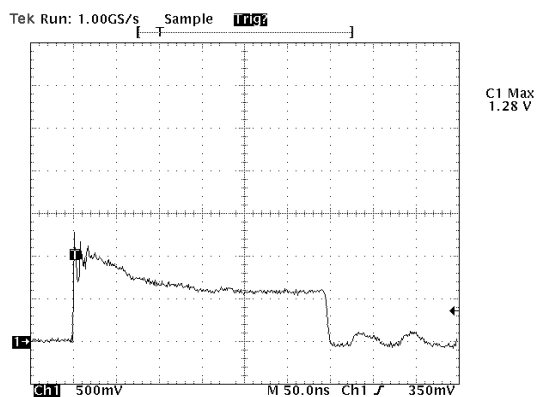
Typical Resistance vs. Temperature



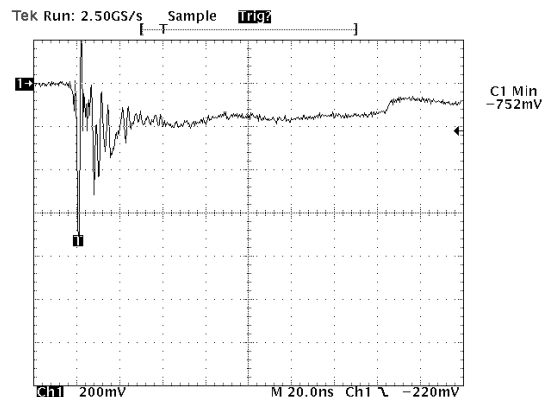
Capacitance vs. Reverse Voltage



ESD Clamping (+8kV Contact)



ESD Clamping (-8kV Contact)



Applications Information

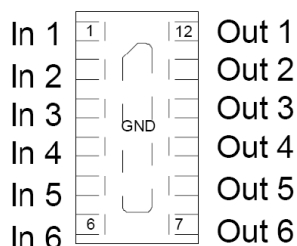
Device Connection

The UM6411 is comprised of six identical circuits each consisting of a low pass filter for EMI/RFI suppression and dual TVS diodes for ESD protection. The device is in a 12-pin DFN package. Electrical connection is made to the 12 pins located at the bottom of the device. A center tab serves as the ground connection. The device has a flow through design for easy layout. Pin connections are noted in Figure 1. All path lengths should be kept as short as possible to minimize the effects of parasitic inductance in the board traces. Recommendations for the ground connection are given below.

Ground Connection Recommendation

Parasitic inductance present in the board layout will affect the filtering performance of the device. As frequency increases, the effect of the inductance becomes more dominant. This effect is given by Equation 1.

Figure 1 - Pin Identification and Configuration (Top Side View)



Pin	Identification
1 - 6	Input Lines
7 - 12	Output Lines
Center Tab	Ground

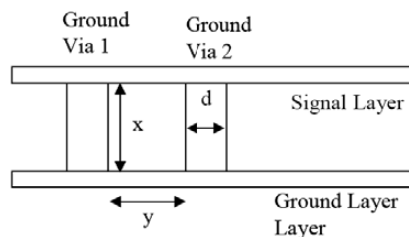
Equation 1: The Impedance of an Inductor at Frequency XLF

$$X_{LF}(L, f) = 2 \times \pi \times f \times L$$

Where:
L = Inductance (H)
f = Frequency (Hz)

Via connections to the ground plane form rectangular wire loops or ground loop inductance as shown in Figure 2. Ground loop inductance can be reduced by using multiple vias to make the connection to the ground plane. Bringing the ground plane closer to the signal layer (preferably the next layer) also reduces ground loop inductance. Multiple vias in the device ground pad will result in a lower inductive ground loop over two exterior vias. Vias with a diameter d are separated by a distance y run between layers separated by a distance x. The inductance of the loop path is given by Equation 2. Thus, decreasing distance x and y will reduce the loop inductance and result in better high frequency filter characteristics.

Figure 2 - Inductance of Rectangular Wire Loops



Equation 2: Inductance of Rectangular Wire Loop

$$L_{RECT}(d, x, y) = 10.16 \times 10^{-9} * \left[x * \ln \left[\frac{2+y}{d} \right] + y * \ln \left[\frac{2+x}{d} \right] \right]$$

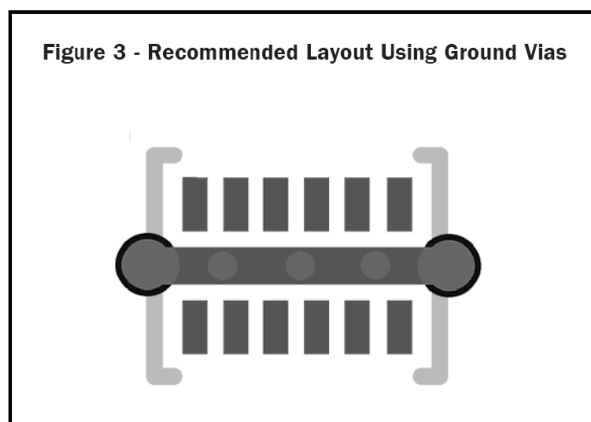
Where:

d = Diameter of the wire (in)

x = Length of wire loop (in)

y = Breath of wire loop (in)

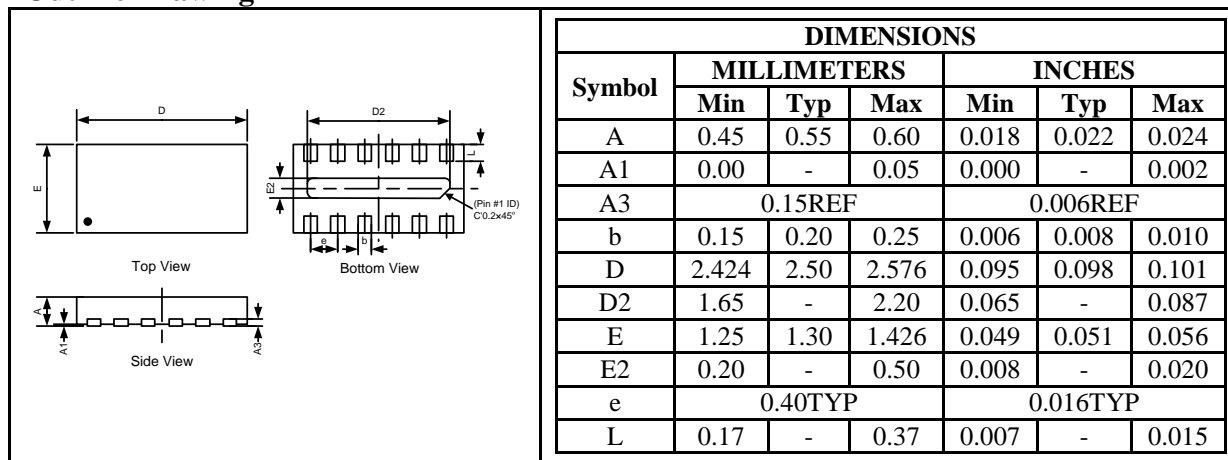
Figure 3 shows the recommended device layout. The ground pad vias have a diameter of 0.008 inches (0.20mm) while the two external vias have a diameter of 0.010 inches (0.250mm). The internal vias are spaced approximately evenly from the center of the pad. The designer may choose to use more vias with a smaller diameter (such as 0.005 inches or 0.125mm) since changing the diameter of the via will result in little change in inductance (i.e. the log function in Equation 2 is highly insensitive to parameter d).



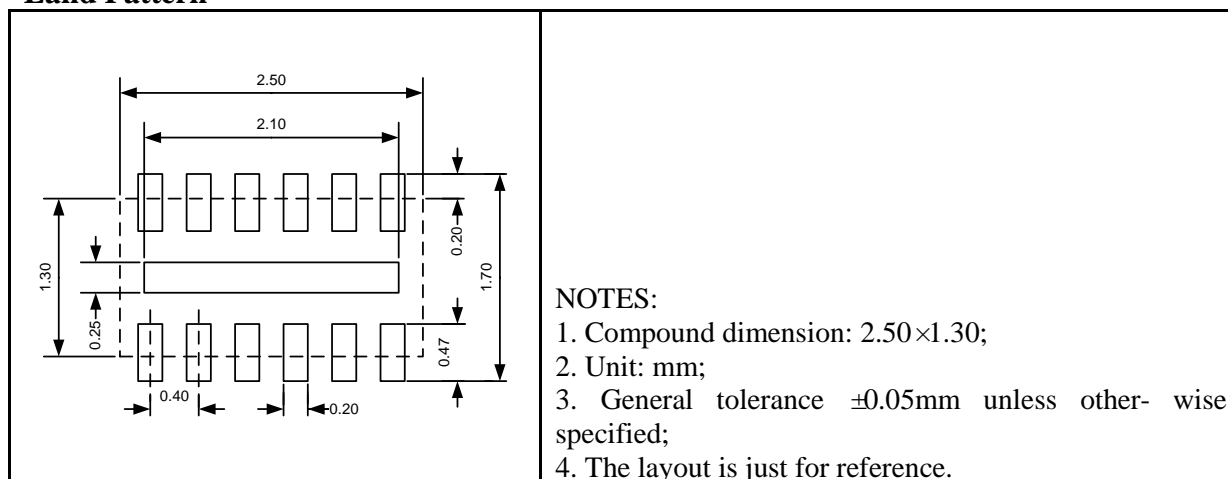
Package Information

UM6411: DFN12 2.5×1.3

Outline Drawing



Land Pattern



Tape and Reel Orientation



GREEN COMPLIANCE

Union Semiconductor is committed to environmental excellence in all aspects of its operations including meeting or exceeding regulatory requirements with respect to the use of hazardous substances. Numerous successful programs have been implemented to reduce the use of hazardous substances and/or emissions.

All Union components are compliant with the RoHS directive, which helps to support customers in their compliance with environmental directives. For more green compliance information, please visit:

http://www.union-ic.com/index.aspx?cat_code=RoHSDeclaration

IMPORTANT NOTICE

The information in this document has been carefully reviewed and is believed to be accurate. Nonetheless, this document is subject to change without notice. Union assumes no responsibility for any inaccuracies that may be contained in this document, and makes no commitment to update or to keep current the contained information, or to notify a person or organization of any update. Union reserves the right to make changes, at any time, in order to improve reliability, function or design and to attempt to supply the best product possible.