四通道、低电容ESD保护二极管阵列

UM5404EEDF *DFN6 1.6×1.6*

描述

UM5404EEDF 浪涌额定二极管阵列是专为保护高速数据传输接口而设计。该系列专门保护连接到数据线和传输线上的敏感元件，使其免受静电放电（ESD）、快速瞬态电流（EFT）和雷击引起的过压损坏。

该器件采用独特设计，将浪涌额定、低电容的转向二极管和一个TVS二极管集成在一个封装中。在瞬态条件下，转向二极管会将瞬态电压导向电源线的正极或接地端。内部TVS二极管可防止电源线上出现过压，从而保护所有下游元件。

UM5404EEDF 具有1pF的低典型电容，并在2GHz频率下几乎无插入损耗。因此，该器件非常适合保护 USB2.0、Firewire、DVI 和千兆以太网接口等高速数据线。

UM5404EEDF的低电容阵列配置允许用户保护四条高速数据或传输线路。低电感结构最大程度地减少了大浪涌电流时的过冲电压。该器件针对便携式电子设备的ESD保护进行了优化，可满足IEC 61000-4-2标准的第4级静电抗扰度要求：±15kV 空气间隙放电和 ±8kV 接触放电。

应用

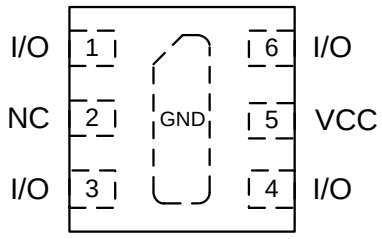
- USB 2.0
- USB OTG
- 10/100/1000Mbit 以太网
- 显示器和平板
- 显示器数字视频接口（DVI）
- 高清多媒体接口 (HDMI)
- SIM 端口
- IEEE 1394 火线端口

特性

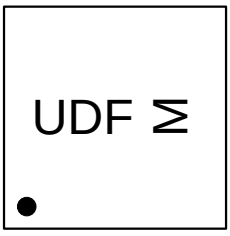
- 高速数据线瞬态保护，符合IEC 61000-4-2标准：
  ±20kV（空气间隙放电），±12kV（接触放电）
  符合IEC 61000-4-4 (EFT)标准：40A (5/50ns)
  符合IEC 61000-4-5(Lighting)标准：10A (8/20μs)
- 带内部TVS二极管的浪涌额定二极管阵列
- 最多可保护四条I/O线和电源线
- 适用于高速接口的低电容特性（<1pF），频率高达2.0GHz无插入损耗
- 低漏电流和钳位电压
- 低工作电压：5.0V

引脚配置

顶部视图

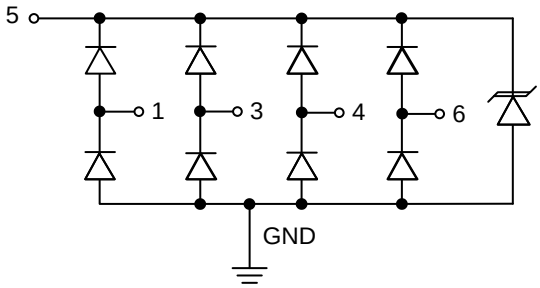


(Top View)



M: Month Code
UM5404EEDF
DFN6 1.6×1.6

Circuit Diagram



Pin Configurations

Pin Number	Symbol	Function
1, 3, 4, 6	I/O	Input/Output Lines
2	NC	Not Connected
5	VCC	Supply Voltage
Center Tab	GND	Ground

Ordering Information

Part Number	Working Voltage	Packaging Type	Channel	Marking Code	Shipping Qty
UM5404EEDF	5.0V	DFN6 1.6×1.6	4	UDF	3000pcs/7 Inch Tape & Reel

Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Peak Pulse Power (t_P=8/20μs)	P_{pk}	200	Watts
Peak Pulse Current (t_P=8/20μs)	I_{PP}	10	A
Peak Pulse Current (t_P=5/50ns)	I_{PP}	40	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	±20 ±12	kV
Operating Temperature	T_J	-55 to +125	℃
Storage Temperature	T_{STG}	-55 to +150	℃

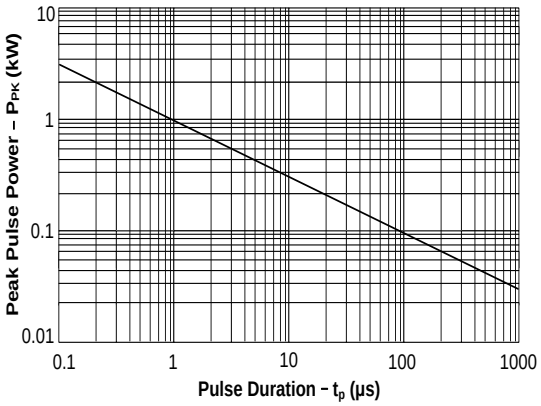
Electrical Characteristics (Note 1)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Reverse Stand-Off Voltage	V_{RWM}	VCC to GND			5.0	V
Reverse Breakdown Voltage	V_{BR}	I_T=1mA, VCC to GND	6.0			V
Reverse Leakage Current	I_R	V_{RWM}=5V, VCC to GND			2	μA
Clamping Voltage	V_C	I_{PP}=1A, 8/20μs Any I/O Pin to GND		8	10	V
Clamping Voltage	V_C	I_{PP}=5A, 8/20μs Any I/O Pin to GND		12	15	V
Junction Capacitance	C_j	V_R=0V, f=1MHz Any I/O Pin to GND			2	pF
		V_R=0V, f=1MHz , Between I/O Pins			1	pF
		V_R=0V, f=1MHz VCC to GND		60		pF
		V_R=2.5V, f=1MHz VCC to GND		40		pF
Reverse Recovery Time	Trr	Any I/O Pin to VCC		130		ns
		GND to VCC		300		ns
		GND to any I/O Pin		400		ns

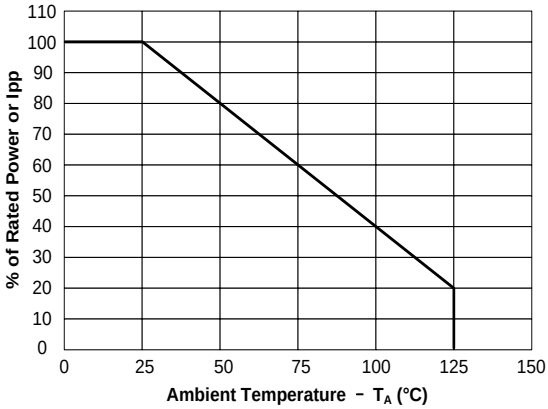
Note 1: I/O pins are pin 1, 3, 4, and 6.

Typical Operating Characteristics

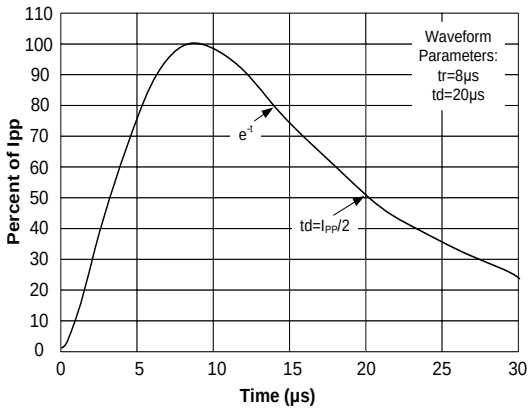
Non-Repetitive Peak Pulse Power vs. Pulse Time



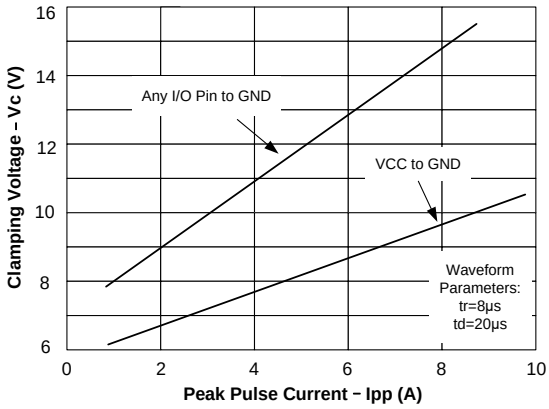
Power Derating Curve



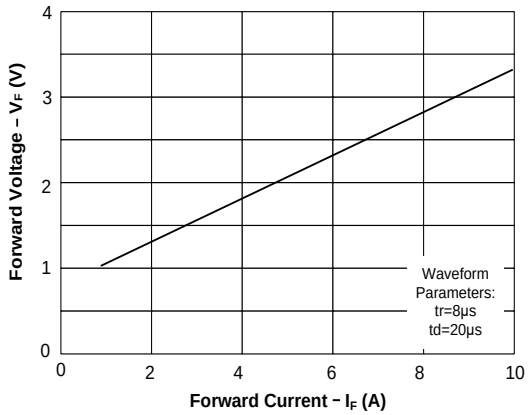
Pulse Waveform



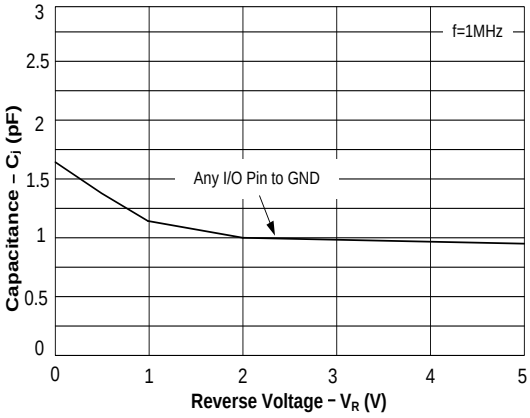
Clamping Voltage vs. Peak Pulse Current



Forward Voltage vs. Forward Current

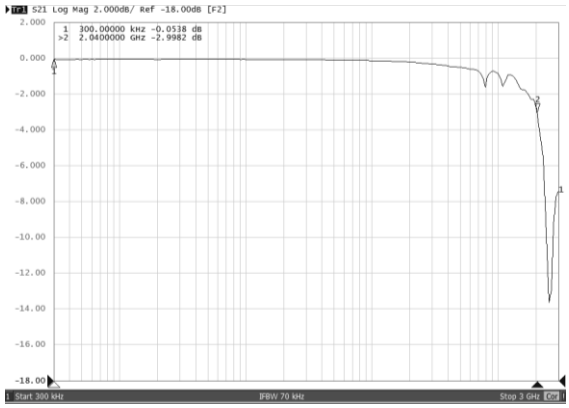


Junction Capacitance vs. Reverse Voltage

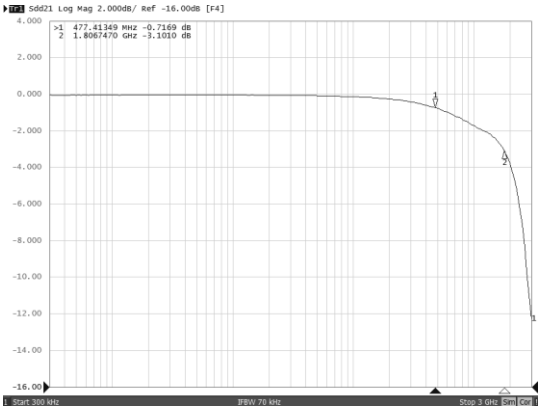


Typical Operating Characteristics (Continued)

Single End Bandwidth



Differential Bandwidth



Crosstalk

Applications Information

Device Connection Options for Protection of Four High-Speed Data Lines

This device is designed to protect four data lines by clamping them to a fixed reference. When the voltage on the protected line exceeds the reference voltage the steering diodes are forward biased, conducting the transient current away from the sensitive circuitry. Data lines are connected at I/O pins. The center GND pin should be connected directly to a ground plane. The path length is kept as short as possible to minimize parasitic inductance. NC pin is not connected. The positive reference is connected at VCC pin. The options for connecting the positive reference are as follows:

1. To protect data lines and the power line, connect VCC pin directly to the positive supply rail (VCC). In this configuration the data lines are referenced to the supply voltage. The internal TVS diode prevents over-voltage on the supply rail. See Figure 1.
2. In applications where the supply rail does not exit the system, the internal TVS may be used as the reference. In this case, VCC pin is not connected. The steering diodes will begin to conduct when the voltage on the protected line exceeds the working voltage of the TVS (plus one diode drop).
3. In applications where complete supply isolation is desired, the internal TVS is again used as the reference and VCC is connected to one of the I/O inputs. An example of this configuration is the protection of a SIM port. The Clock, Reset, I/O, and VCC lines are connected at I/O pins. GND pin is connected to ground, NC and VCC pins are not connected. See Figure 2.

Protection of Four Data Lines and Power Supply Line

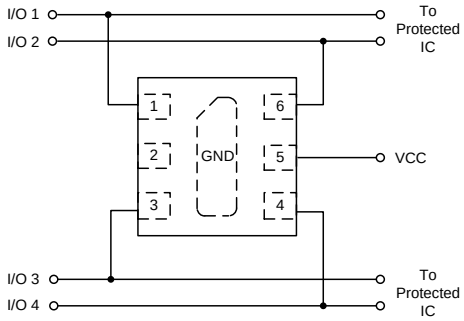


Figure 1

Protection of Four Data Lines Using Internal TVS Diode as Reference

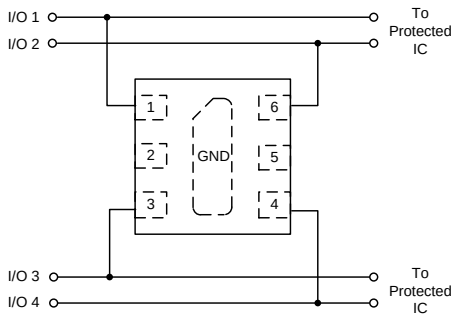


Figure 2

Universal Serial Bus ESD Protection

The UM5404EEDF may also be used to protect the USB ports on monitors, computers, peripherals or portable systems. Each device will protect up to two USB ports (Figure 3). When the voltage on the data lines exceed the bus voltage (plus one diode drop), the internal rectifiers are forward biased conducting the transient current away from the protected controller chip. The TVS diode directs the surge to ground. The TVS diode also acts to suppress ESD strikes directly on the voltage bus. Thus, both power and data pins are protected with a single device.

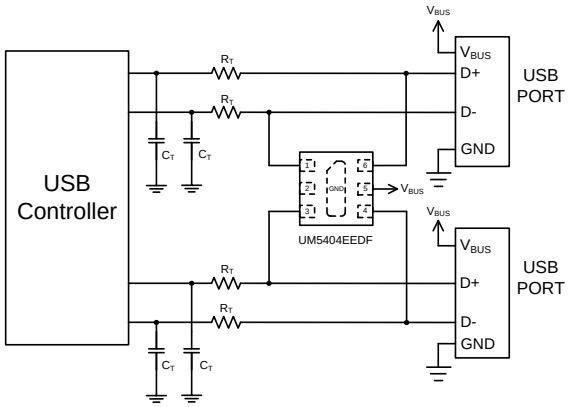


Figure 3 Dual USB Port Protection

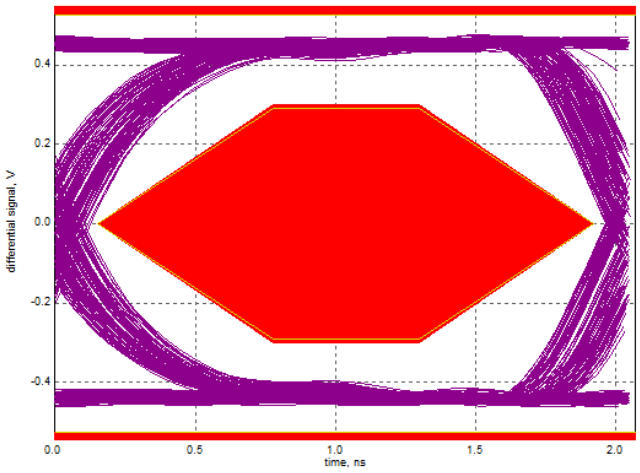


Figure 4 USB Eye Diagram

Note: Figure 4 is tested by the MSO9254A oscilloscope of Agilent including E2678 probe, 1169 differential probe and E2645B-66401 fixture, when the chip is linked into the data line.

10/100 Ethernet Protection

Ethernet ICs are vulnerable to damage from electrostatic discharge (ESD). The internal protection in the PHY chip, if any, often is not enough due to the high energy of the discharges specified by IEC61000-4-2. If the discharge is catastrophic, it will destroy the protected IC. If it is less severe, it will cause latent failures that are very difficult to find.

10/100 Ethernet operates at 125MHz clock over a twisted pair interface. In a typical system, the twisted pair interface for each port consists of two differential signal pairs: one for the transmitter and one for the receiver, with the transmitter input being the most sensitive to damage. The fatal discharge occurs differentially across the transmitter or receiver line pair and is capacitively coupled through the transformer to the Ethernet chip. Figure 5 shows how to design the UM5404EEDF on the line side of a 10/100 ethernet port to provide differential mode protection. The common mode isolation of the transformer will provide common mode protection to the rating of the transformer isolation which is usually >1.5kV. If more common mode protection is needed, figure 6 shows how to design the UM5404EEDF on the IC side of the 10/100 Ethernet circuit to provide differential and common mode protection. The UM5404EEDF can not be grounded on the line side because the hi-pot test requires the line side not to be grounded.

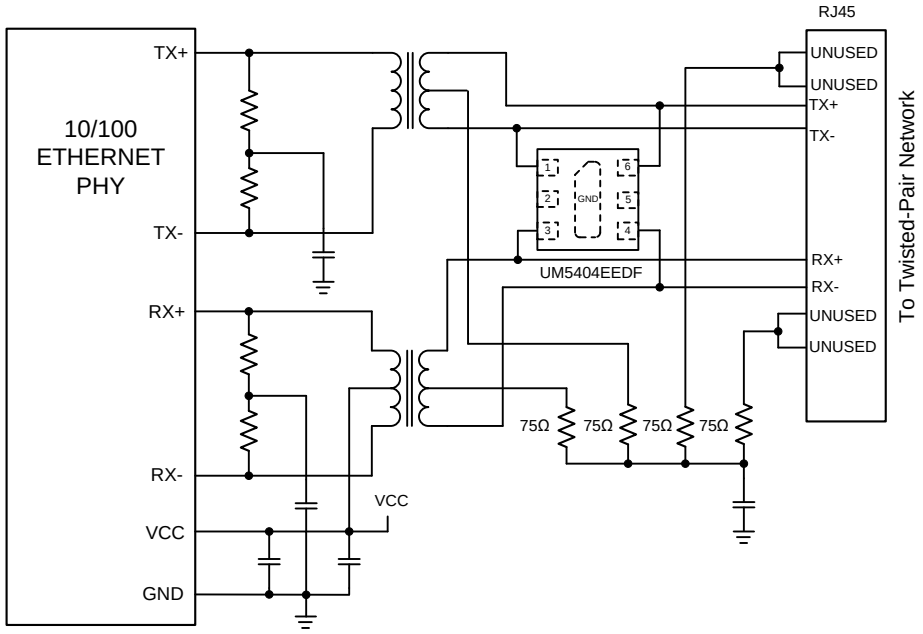


Figure 5 10/100 Ethernet Differential Protection

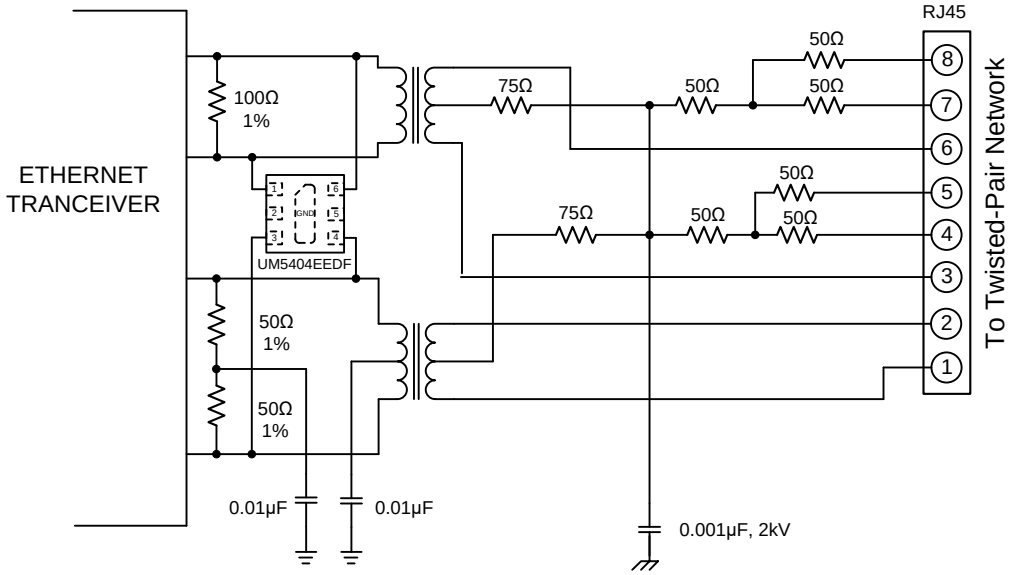


Figure 6 10/100 Ethernet Differential and Common Mode Protection

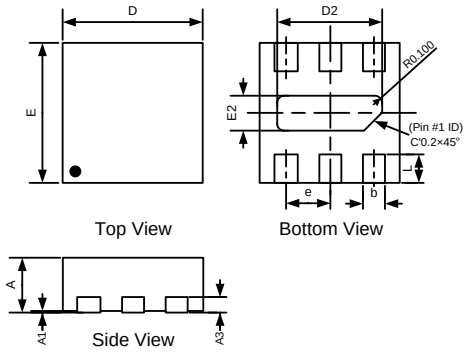
Matte Tin Lead Finish

Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. In addition, unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation of the solder joint.

Package Information

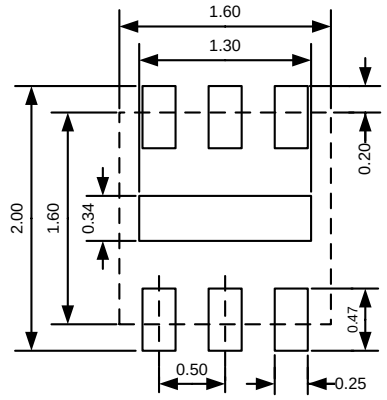
UM5404EEDF DFN6 1.6×1.6

Outline Drawing



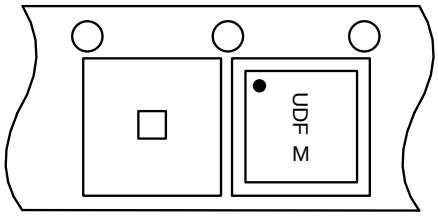
DIMENSIONS						
Symbol	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	0.50	0.575	0.605	0.020	0.023	0.024
A1	0.00	-	0.05	0.000	-	0.002
A3	0.15REF			0.006REF		
b	0.20	0.25	0.30	0.008	0.010	0.012
D	1.524	1.60	1.676	0.060	0.063	0.066
D2	0.90	-	1.36	0.035	-	0.054
E	1.524	1.60	1.676	0.060	0.063	0.066
E2	0.30	-	0.65	0.012	-	0.026
e	0.50TYP			0.020TYP		
L	0.175	-	0.426	0.007	-	0.017

Land Pattern



NOTES:
1. Compound dimension: 1.60×1.60;
2. Unit: mm;
3. General tolerance ±0.05mm unless otherwise specified;
4. The layout is just for reference.

Tape and Reel Orientation



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