

四通道、低电容ESD保护二极管阵列

UM5204EEAF SC70-6/SC88/SOT363

UM5204EEBF SC89-6/SOT563/SOT666

UM5204EECF TSOP-6/SOT23-6

描述

UM5204EEXF系列浪涌额定二极管阵列专为高速数据接口的防护设计，其核心功能是保护连接在数据及传输线路上的敏感元件，使其免受静电放电（ESD）引发的过压损坏。

该器件采用独特设计，将浪涌额定、低电容的转向二极管和一个 TVS二极管集成在一个封装中。在瞬态条件下，转向二极管会将瞬态电压导向电源线的正极或接地端。内部 TVS 二极管可防止电源线上出现过压，从而保护所有下游元件。

UM5204EEXF的低电容阵列配置允许用户保护四条高速数据或传输线路。低电感结构最大程度地减少了大浪涌电流时的过冲电压。该器件针对便携式电子设备的ESD保护进行了优化，可满足IEC 61000-4-2标准的第4级静电抗扰度要求：±15kV 空气间隙放电和 ±8kV 接触放电。

应用

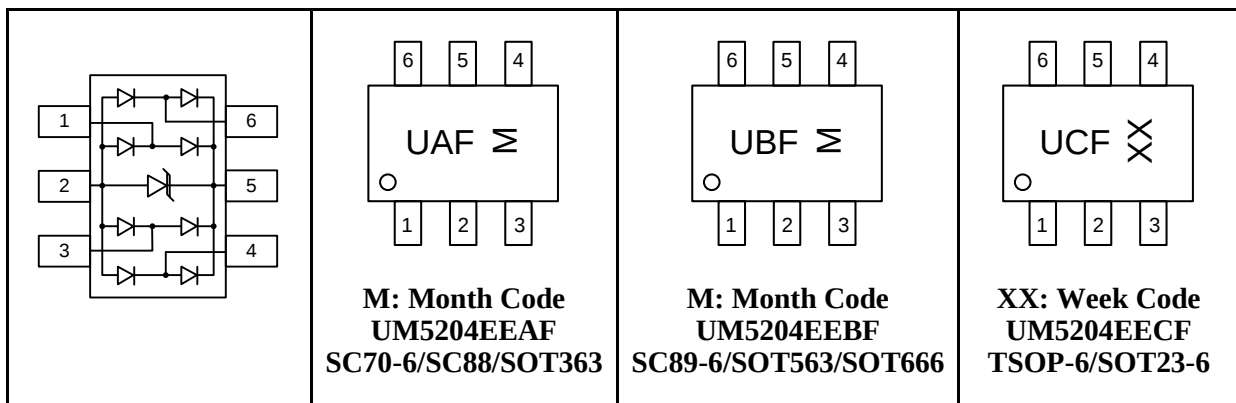
- USB 2.0
- USB OTG
- 显示器和平板
- 显示器数字视频接口（DVI）
- 高清多媒体接口（HDMI）
- SIM 端口
- IEEE 1394 火线端口

特性

- 高速数据线瞬态保护，符合IEC 61000-4-2标准：±15kV（空气间隙放电），±8kV（接触放电）
- 带内部 TVS 二极管的浪涌额定二极管阵列
- 最多可保护四条 I/O 线和电源线
- 适用于高速接口的低电容特性（<2pF）
- 频率高达2.0GHz无插入损耗
- 低漏电流和钳位电压
- 反向工作电压：5.0V
- 固态硅雪崩技术

引脚配置

顶部视图



Ordering Information

Part Number	Working Voltage	Packaging Type	Channel	Marking Code	Shipping Qty
UM5204EEAF	5.0V	SC70-6/SC88/SOT363	4	UAF	3000pcs/7 Inch Tape & Reel
UM5204EEBF		SC89-6/SOT563/SOT666		UBF	
UM5204EECF		TSOP-6/SOT23-6		UCF	

Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Peak Pulse Power ($t_p=8/20\mu s$)	P_{pk}	150	Watts
Peak Pulse Current ($t_p=8/20\mu s$)	I_{pp}	6	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	± 15 ± 8	kV
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

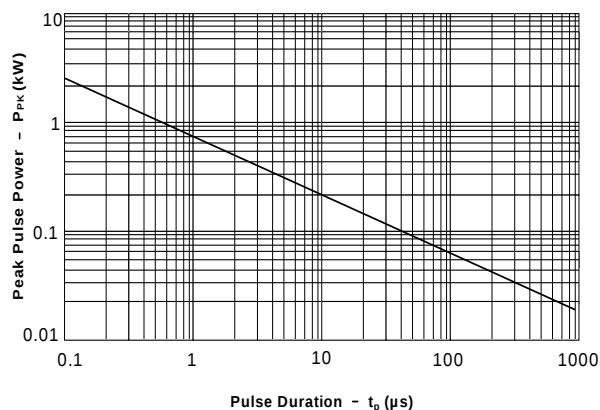
Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Reverse Stand-Off Voltage	V_{RWM}				5.0	V
Reverse Breakdown Voltage	V_{BR}	$I_T=1mA$, Pin 5 to 2	6.0			V
Reverse Leakage Current	I_R	$V_{RWM}=5V$, $T=25^\circ C$ Pin 5 to 2			2	μA
Clamping Voltage	V_C	$I_{pp}=1A$, $8/20\mu s$ Any Pin to Pin 2			15	V
Clamping Voltage	V_C	$I_{pp}=6A$, $8/20\mu s$ Any Pin to Pin 2			25	V
Junction Capacitance	C_j	$V_R=0V$, $f=1MHz$ Any I/O Pin to Pin 2 (Note 1)			2	pF
		$V_R=0V$, $f=1MHz$ Between I/O Pins (Note 1)			1	pF

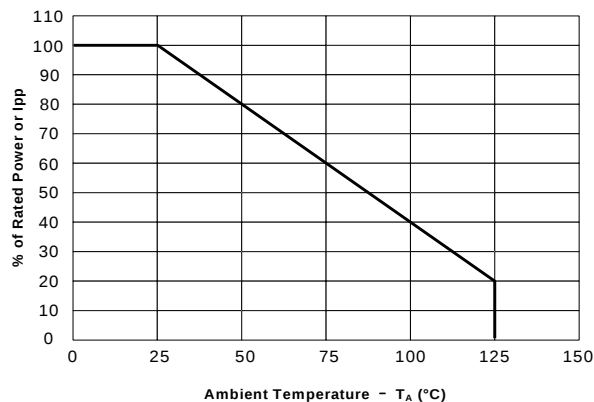
Note 1: I/O pins are pin 1, 3, 4, and 6

Typical Operating Characteristics

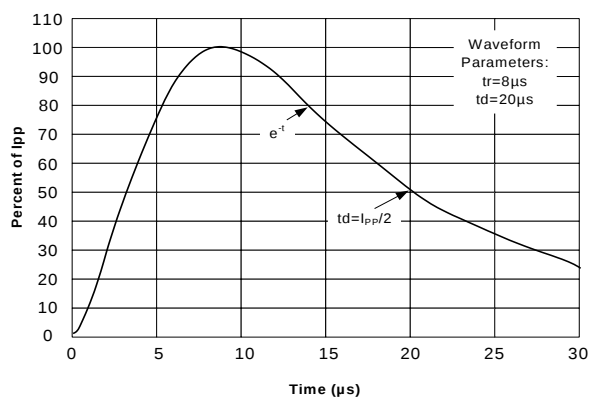
Non-Repetitive Peak Pulse Power vs. Pulse Time



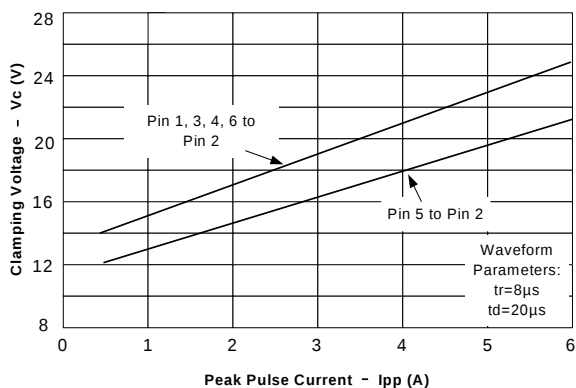
Power Derating Curve



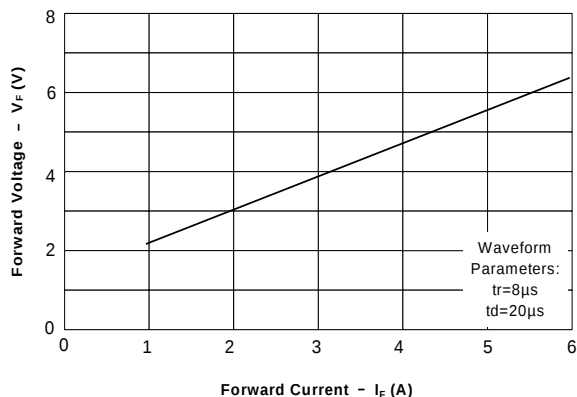
Pulse Waveform



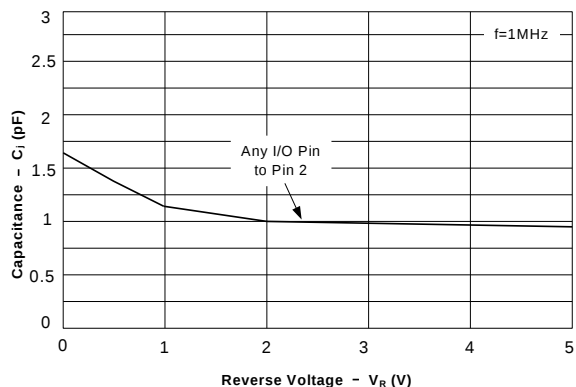
Clamping Voltage vs. Peak Pulse Current



Forward Voltage vs. Forward Current



Junction Capacitance vs. Reverse Voltage

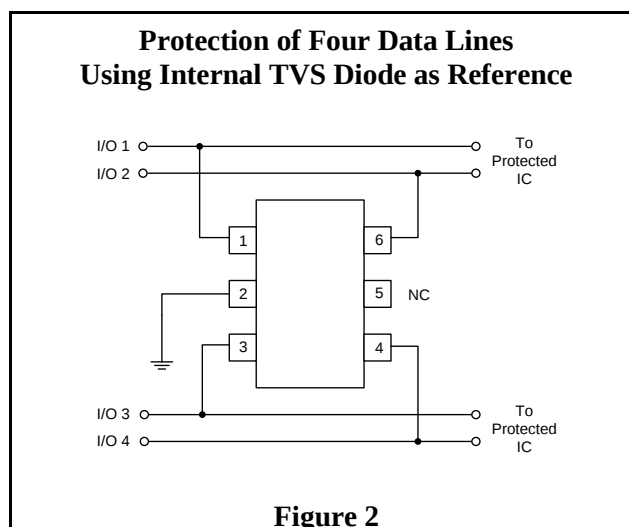
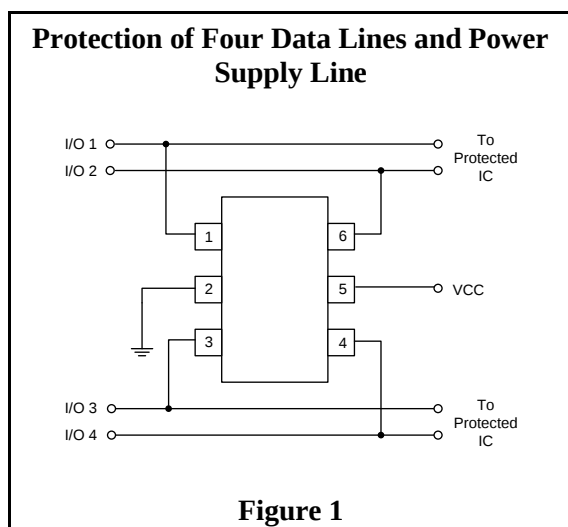


Applications Information

Device Connection Options for Protection of Four High-Speed Data Lines

This device is designed to protect data lines by clamping them to a fixed reference. When the voltage on the protected line exceeds the reference voltage the steering diodes are forward biased, conducting the transient current away from the sensitive circuitry. Data lines are connected at pins 1, 3, 4 and 6. Pin 2 should be connected directly to a ground plane. The path length is kept as short as possible to minimize parasitic inductance. The positive reference is connected at pin 5. The options for connecting the positive reference are as follows:

1. To protect data lines and the power line, connect pin 5 directly to the positive supply rail (VCC). In this configuration the data lines are referenced to the supply voltage. The internal TVS diode prevents over-voltage on the supply rail. See Figure 1.
2. In applications where the supply rail does not exit the system, the internal TVS may be used as the reference. In this case, pin 5 is not connected. The steering diodes will begin to conduct when the voltage on the protected line exceeds the working voltage of the TVS (plus one diode drop).
3. In applications where complete supply isolation is desired, the internal TVS is again used as the reference and VCC is connected to one of the I/O inputs. An example of this configuration is the protection of a SIM port. The Clock, Reset, I/O, and VCC lines are connected at pins 1, 3, 4, and 6. Pin 2 is connected to ground and pin 5 is not connected. See Figure 2.



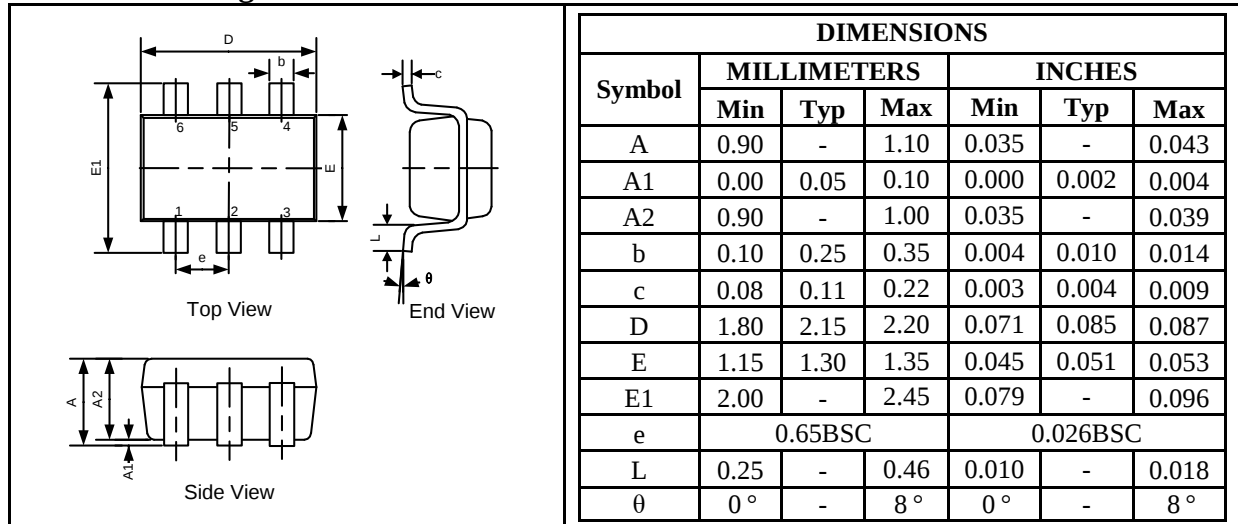
Matte Tin Lead Finish

Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. In addition, unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation of the solder joint.

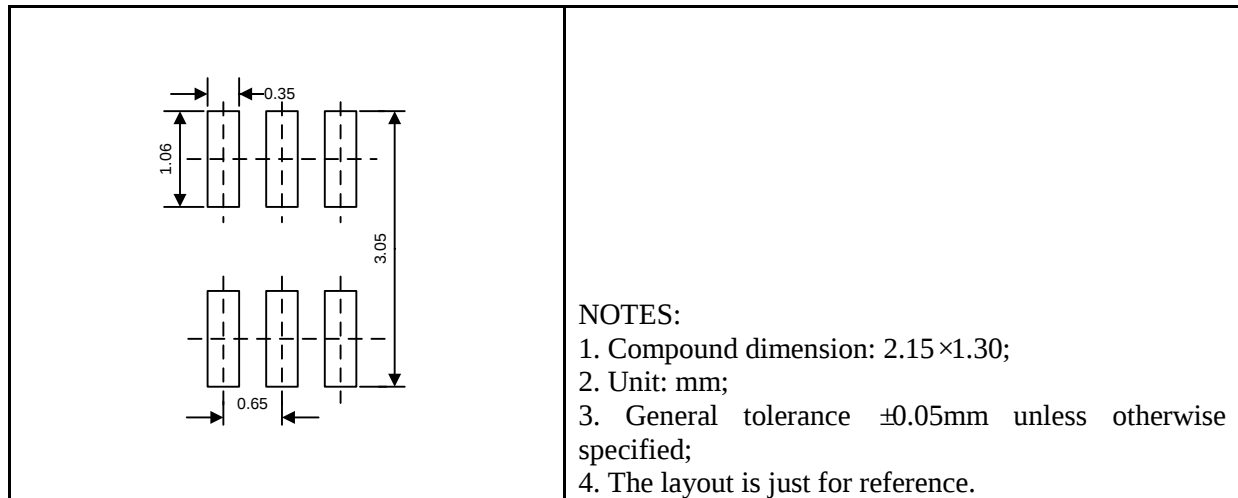
Package Information

UM5204EEAF SC70-6/SC88/SOT363

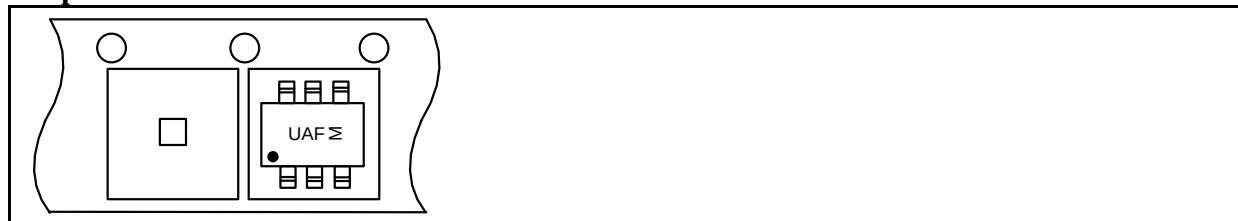
Outline Drawing



Land Pattern

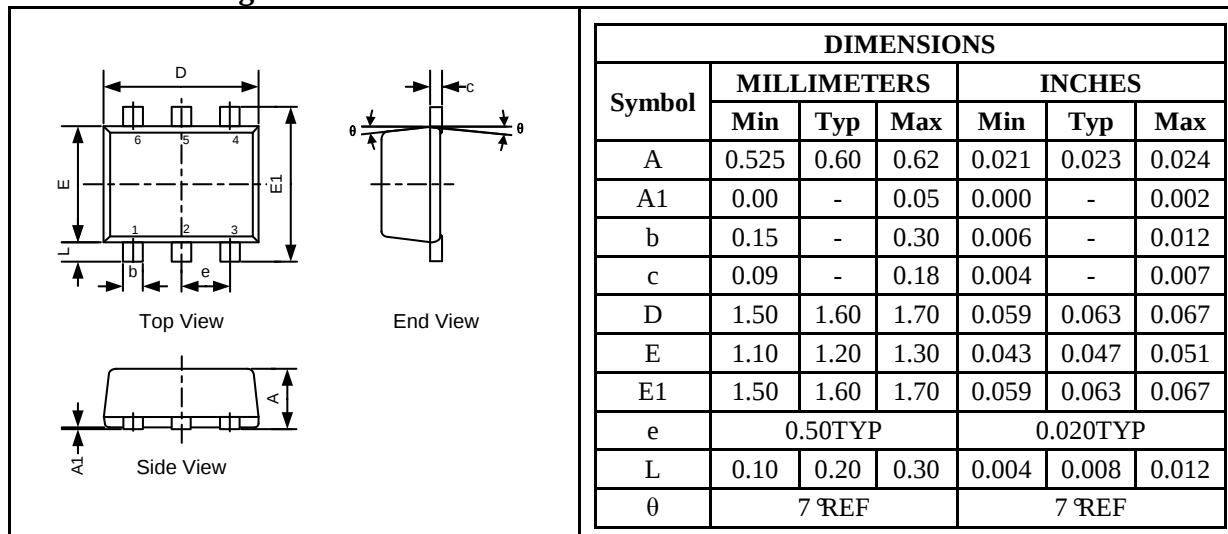


Tape and Reel Orientation

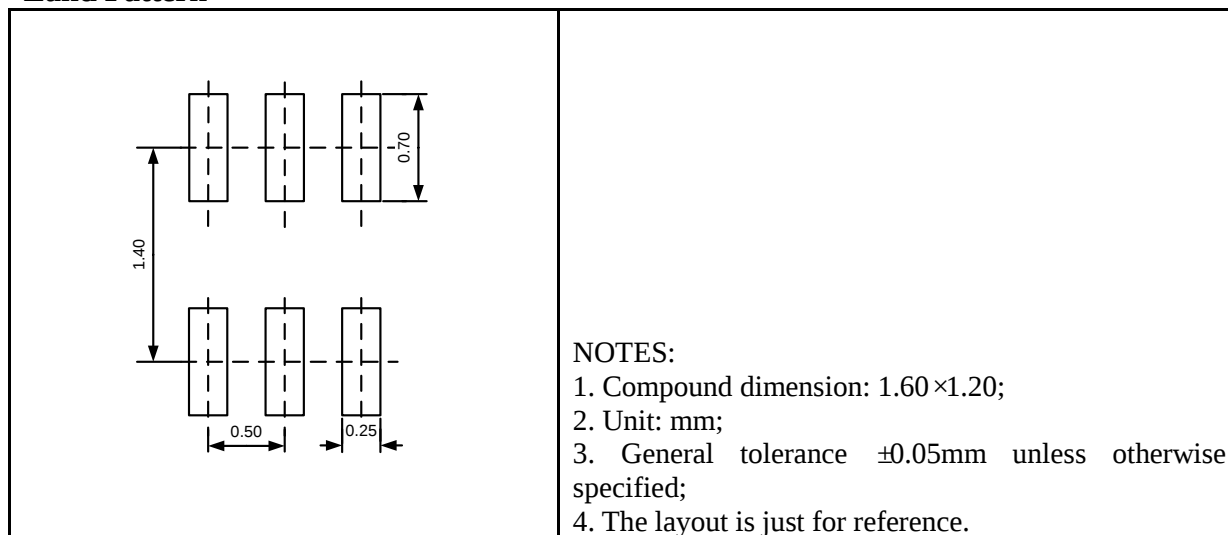


UM5204EEBF SC89-6/SOT563/SOT666

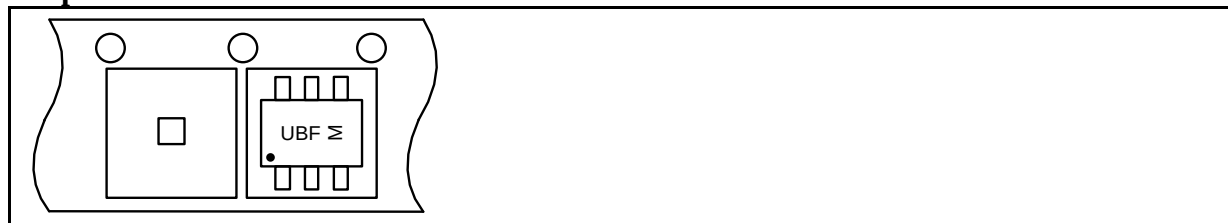
Outline Drawing



Land Pattern

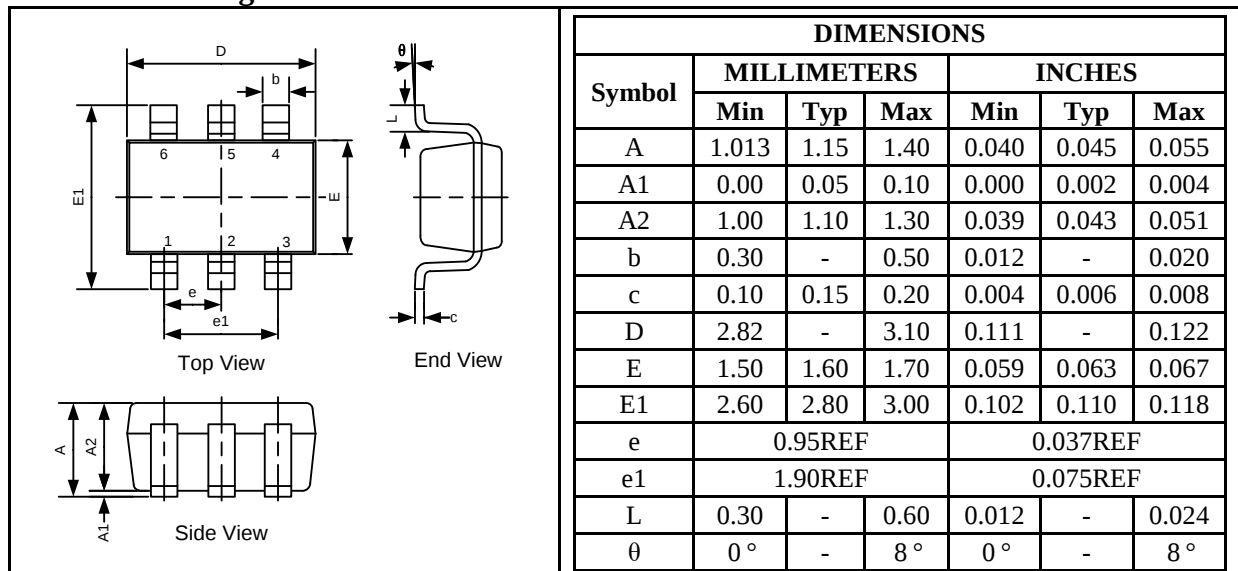


Tape and Reel Orientation

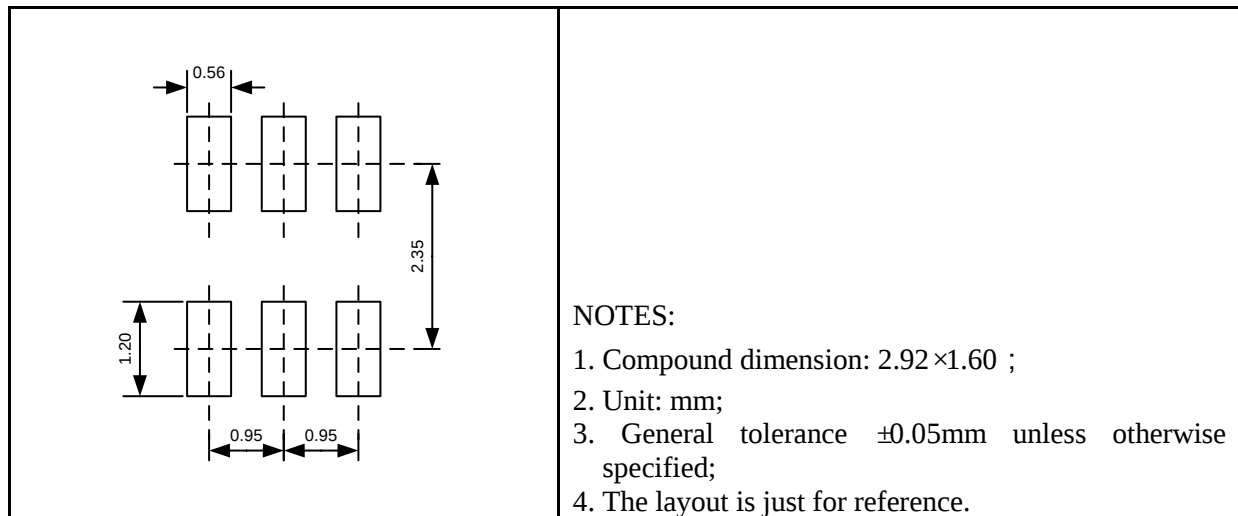


UM5204EECF TSOP-6/SOT23-6

Outline Drawing



Land Pattern



Tape and Reel Orientation



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http://www.union-ic.com/index.aspx?cat_code=RoHSDeclaration

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