

双通道、低电容ESD保护二极管阵列

UM5202EEDF SOT143

描述

UM5202EEDF系列浪涌额定二极管阵列专为高速数据接口的防护设计，其核心功能是保护连接在数据及传输线路上的敏感元件，使其免受静电放电（ESD）引发的过压损坏。

该器件采用独特设计，将浪涌额定、低电容的转向二极管和一个TVS二极管集成在一个封装中。在瞬态条件下，转向二极管会将瞬态电压导向电源线的正极或接地端。内部TVS二极管可防止电源线上出现过压，从而保护所有下游元件。

UM5202EEDF 的低电容阵列配置允许用户保护二条高速数据或传输线路。低电感结构最大程度地减少了大浪涌电流时的过冲电压。该器件针对便携式电子设备的ESD保护进行了优化，可满足IEC 61000-4-2标准的第4级静电抗扰度要求： $\pm 15\text{kV}$ 空气间隙放电和 $\pm 8\text{kV}$ 接触放电。

应用

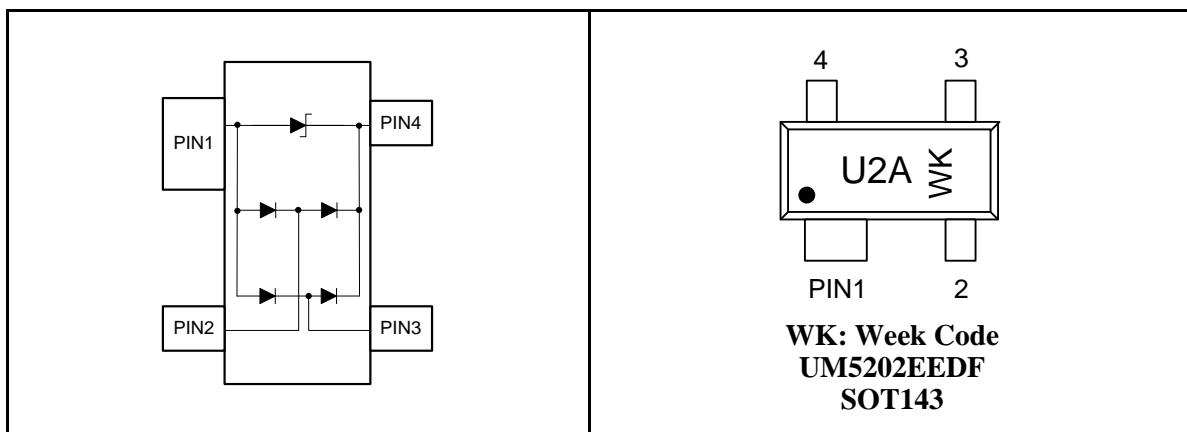
- USB 2.0
- USB OTG
- 显示器和平板
- 显示器数字视频接口（DVI）
- 高清多媒体接口（HDMI）
- SIM 端口
- IEEE 1394 火线端口

特性

- 高速数据线瞬态保护，符合IEC 61000-4-2标准：
 - $\pm 15\text{kV}$ （空气间隙放电）
 - $\pm 8\text{kV}$ （接触放电）
- 带内部TVS二极管的浪涌额定二极管阵列
- 保护二条I/O线和电源线
- 适用于高速接口的低电容特性（ $< 2\text{pF}$ ）
- 至 2.0GHz 时无插入损耗
- 低漏电流和钳位电压
- 反向工作电压：5.0V
- 固态硅雪崩技术

引脚配置

顶部视图



Ordering Information

Part Number	Working Voltage	Packaging Type	Channel	Marking Code	Shipping Qty
UM5202EEDF	5.0V	SOT143	2	U2A	3000pcs/7 Inch Tape & Reel

Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Peak Pulse Power ($t_p=8/20\mu s$)	P_{pk}	150	Watts
Peak Pulse Current ($t_p=8/20\mu s$)	I_{pp}	6	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	± 15 ± 8	kV
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Characteristics (Note 1)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Reverse Stand-Off Voltage	V_{RWM}				5.0	V
Reverse Breakdown Voltage	V_{BR}	$I_T=1mA$, Pin 4 to Pin 1	6.0			V
Reverse Leakage Current	I_R	$V_{RWM}=5V$, $T=25^\circ C$, Pin 4 to Pin 1			2	μA
Clamping Voltage	V_C	$I_{pp}=1A$, $8/20\mu s$, Any Pin to Pin 1			15	V
Clamping Voltage	V_C	$I_{pp}=6A$, $8/20\mu s$, Any Pin to Pin 1			25	V
Junction Capacitance	C_j	$V_R=0V$, $f=1MHz$, Any I/O Pin to Pin 1			2	pF
		$V_R=0V$, $f=1MHz$, Between I/O Pins			1	pF
		$V_R=0V$, $f=1MHz$, Pin 4 to Pin 1		60		pF
		$V_R=2.5V$, $f=1MHz$, Pin 4 to Pin 1		40		pF
Reverse Recovery Time	T_{rr}	Pin 1 to Pin 4		40		ns
		Pin 1 to I/O Pin		160		ns
		Pin 4 to I/O Pin		45		ns

Note 1: I/O pins are pin 2, 3.

Applications Information

Device Connection Options for Protection of Two High-Speed Data Lines

This device is designed to protect data lines by clamping them to a fixed reference. When the voltage on the protected line exceeds the reference voltage the steering diodes are forward biased, conducting the transient current away from the sensitive circuitry. Data lines are connected at pins 2, 3. Pin 1 should be connected directly to a ground plane. The path length is kept as short as possible to minimize parasitic inductance. The positive reference is connected at pin 4. The options for connecting the positive reference are as follows:

1. To protect data lines and the power line, connect pin 4 directly to the positive supply rail (VCC). In this configuration the data lines are referenced to the supply voltage. The internal TVS diode prevents over-voltage on the supply rail.
2. In applications where the supply rail does not exit the system, the internal TVS may be used as the reference. In this case, pin 4 is not connected. The steering diodes will begin to conduct when the voltage on the protected line exceeds the working voltage of the TVS (plus one diode drop).

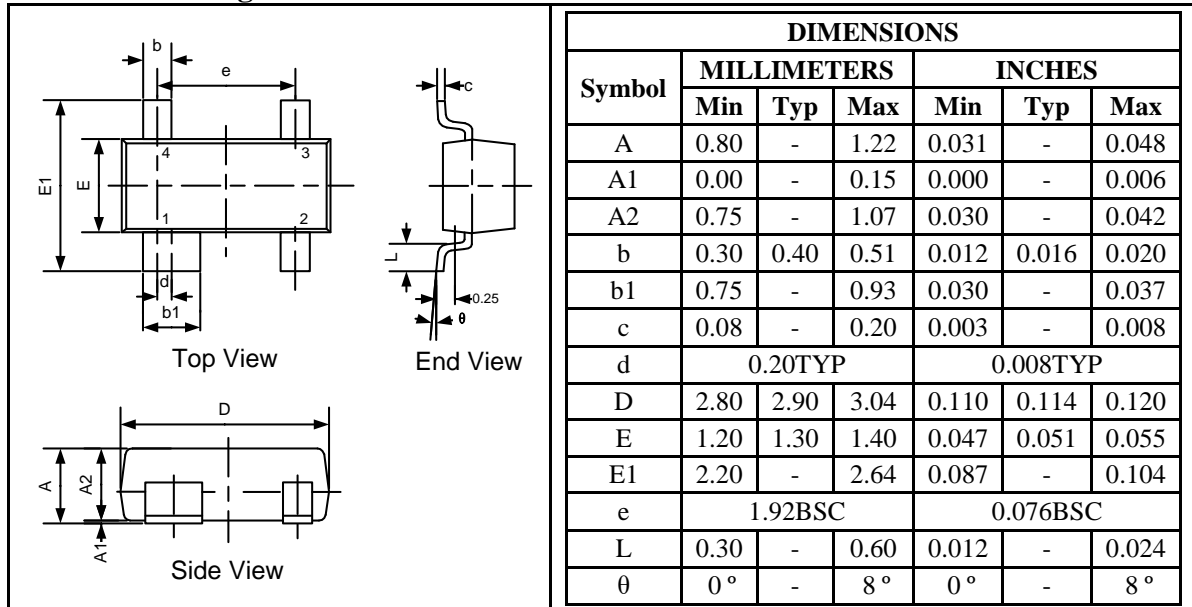
Matte Tin Lead Finish

Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. In addition, unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation of the solder joint.

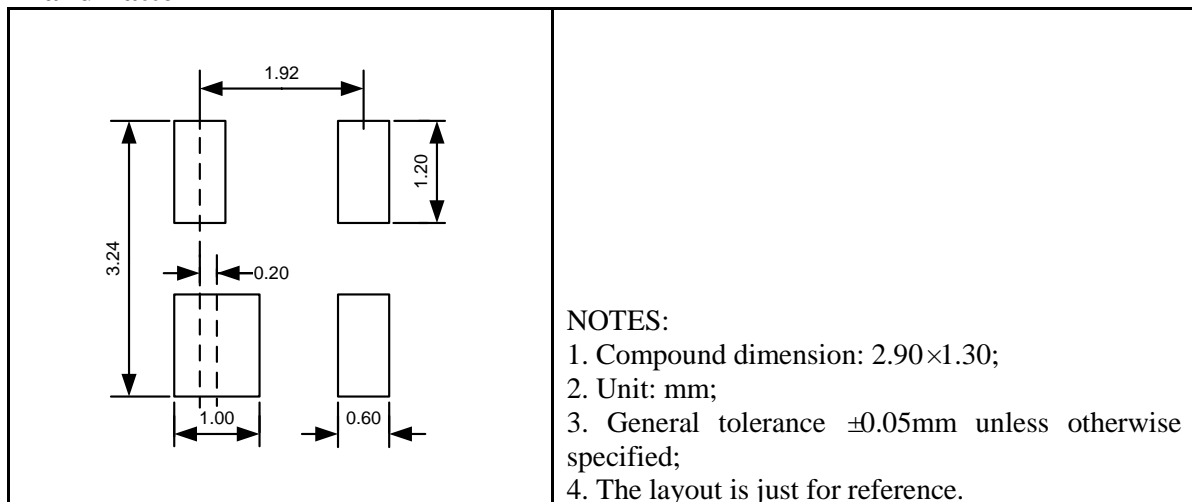
Package Information

UM5202EEDF SOT143

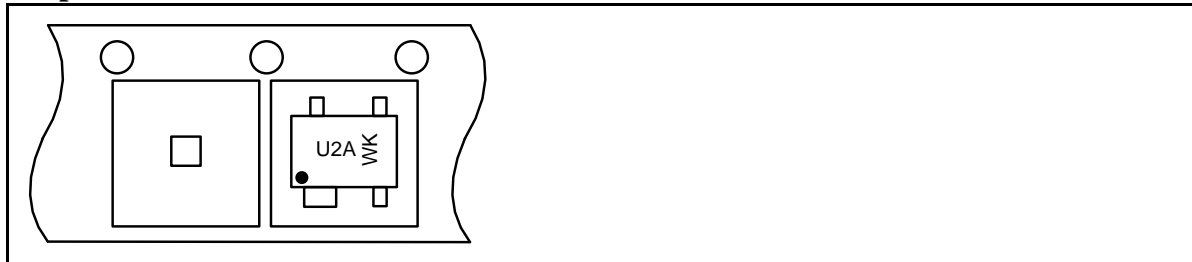
Outline Drawing



Land Pattern



Tape and Reel Orientation



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