

单通道、双向ESD保护二极管 UM5052DA DFN2 0.6×0.3

描述

UM5052DA ESD保护二极管设计用于取代手机、笔记本电脑和PDA等便携式应用中的MLV。与MLV相比,该器件具有板级保护的理想电气特性,例如快速响应时间、较低的工作电压、较低的钳位电压和无器件劣化。UM5052DA ESD保护二极管可保护敏感的半导体元件免受静电放电 (ESD) 和其他瞬态电压事件的损坏或破坏。UM5052DA采用DFN2 0.6mm×0.3mm封装,工作电压为5 V。在不适合采用阵列的应用中,设计人员可以灵活地使用该器件保护一条双向线路。此外,在电路板空间有限的应用中,该器件可采用分散布置的布局方案。该器件可满足IEC 61000-4-2标准的静电放电抗扰度要求: ±30kV 空气间隙放电和 ±30kV接触放电。

应用

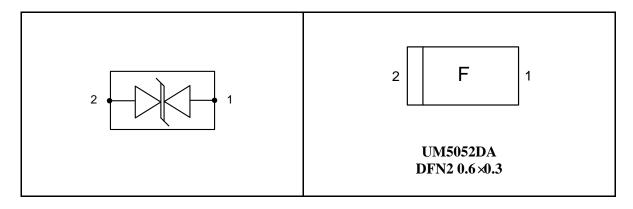
- 手机听筒和配件
- PDA
- 笔记本电脑、台式机和服务器
- 便携式设备
- 无线电话
- 数码相机
- 外围设备
- MP3 播放器

特性

- 数据线瞬态保护,符合IEC 61000-4-2标准: ±30kV(空气间隙放电)、±30kV(接触放电)
- 用于便携式电子设备的小型封装
- ESD保护应用中MLV的合适替代品
- 保护一路I/O或电源线
- 低钳位电压
- 反向工作电压: 5V
- 低漏电流
- 固态硅雪崩技术

引脚配置

顶部视图





Ordering Information

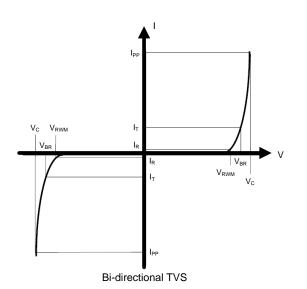
Part Number	Working Voltage	Packaging Type	Packaging Type Channel Marking Code		Shipping Qty
UM5052DA	5.0V	DFN2 0.6×0.3	1	F	8000pcs/7 Inch Tape & Reel

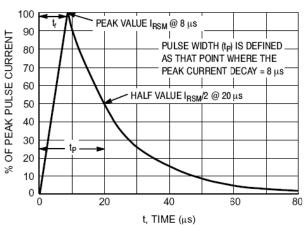
Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Peak Pulse Power (t _P =8/20μs)	P_{PK}	60	Watts
Maximum Peak Pulse Current (t _P =8/20μs)	I_{PP}	5	Amps
Lead Soldering Temperature	T_{L}	260 (10 sec.)	${\mathcal C}$
Operating Temperature	T_{J}	-55 to +125	\mathcal{C}
Storage Temperature	T_{STG}	-55 to +150	$\mathcal C$

Symbol Definition

Parameter	Symbol
Maximum Reverse Peak Pulse Current	I_{PP}
Clamping Voltage @ IPP	$V_{\rm C}$
Working Peak Reverse Voltage	$V_{ m RWM}$
Maximum Reverse Leakage Current @ V _{RWM}	I_R
Breakdown Voltage @ I _T	$ m V_{BR}$
Test Current	I_{T}
Peak Power Dissipation	P_{PK}
Max. Capacitance @ V _R =0V, f=1MHz	С







Electrical Characteristics

(T=25 ℃, Device for 5.0V Reverse Stand-Off Voltage)

Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Reverse Stand-Off Voltage	V_{RWM}				5	V
Reverse Breakdown Voltage	V_{BR}	I _T =1mA	6.5	8.0	8.5	V
Reverse Leakage Current	I_R	$V_{RWM}=5V, T=25 ^{\circ}\text{C}$			1	μΑ
Clamping Voltage	$V_{\rm C}$	$I_{PP}=5A$, $t_P=8/20\mu s$		12		V
Junction Capacitance	C_{J}	$V_R=0V$, $f=1MHz$		7	10	pF
Junction Capacitance	C_{J}	$V_R=2.5V$, $f=1MHz$		6	9	pF

Applications Information

Device Connection Options

UM5052DA ESD protection diode is designed to protect one bidirectional data, I/O, or power supply line from the damage caused by ESD and surge pluses. The device is bidirectional and can be used on lines where the signal polarity is above ground and below ground.

Circuit Board Layout Recommendations for Suppression of ESD

Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

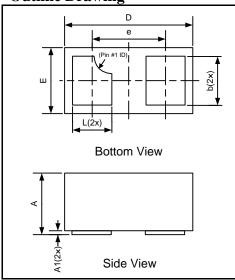
- 1. Place the TVS near the input terminals or connectors to restrict transient coupling.
- 2. Minimize the path length between the TVS and the protected line.
- 3. Minimize all conductive loops including power and ground loops.
- 4. The ESD transient return path to ground should be kept as short as possible.
- 5. Never run critical signals near board edges.
- 6. Use ground planes whenever possible. For multilayer printed-circuit boards, use ground vias.
- 7. Keep parallel signal paths to a minimum.
- 8. Avoid running protection conductors in parallel with unprotected conductor.
- 9. Minimize all printed-circuit board conductive loops including power and ground loops.
- 10. Avoid using shared transient return paths to a common ground point.



Package Information

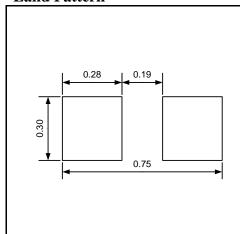
UM5052DA DFN2 0.6×0.3

Outline Drawing



DIMENSIONS						
Gb1	MILLIMETERS			INCHES		
Symbol	Min	Тур	Max	Min	Тур	Max
A	0.27	0.30	0.35	0.011	0.012	0.014
A1	0.00	0.02	0.03	0.000	0.0008	0.0012
b	0.19	0.24	0.29	0.007	0.009	0.011
D	0.595	0.62	0.645	0.023	0.024	0.025
Е	0.295	0.32	0.345	0.012	0.013	0.014
e	0.355TYP			0.014TYP		
L	0.16	0.19	0.23	0.006	0.007	0.009

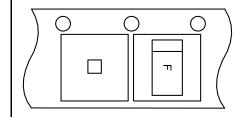
Land Pattern



NOTES:

- 1. Compound dimension: 0.6×0.3;
- 2. Unit: mm;
- 3. General tolerance ± 0.025 mm unless otherwise specified;
- 4. The layout is just for reference.

Tape and Reel Orientation





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