

0.5Ω、低压、双通道单刀双掷 (SPDT) 模拟开关**UM4684H CSP10 2.0×1.5**
UM4684EEUE MSOP10**描述**

UM4684是一款导通电阻小于1Ω (2.7V电源时为0.5Ω)，双通道单刀双掷模拟开关，专为低电压应用设计。

UM4684在整个电压范围内保证导通电阻匹配（2.7V电源时小于0.05Ω）和平坦度（2.7V电源时小于0.2Ω）。此外，逻辑管脚的低电压阈值使UM4684成为连接低压DSP控制信号的理想接口。

UM4684在保证先断后合的功能下，具有快速的开关速度。在开关打开的情况下，所有开关在两个方向上的开关速率相同。关断隔离度和串扰在100kHz时为-69dB。

UM4684采用高密度低压CMOS工艺制造，还具有2000V ESD保护功能。

作为社区和环境的忠实合作伙伴，Union在生产该产品时采用了无铅器件终端。

应用**特性**

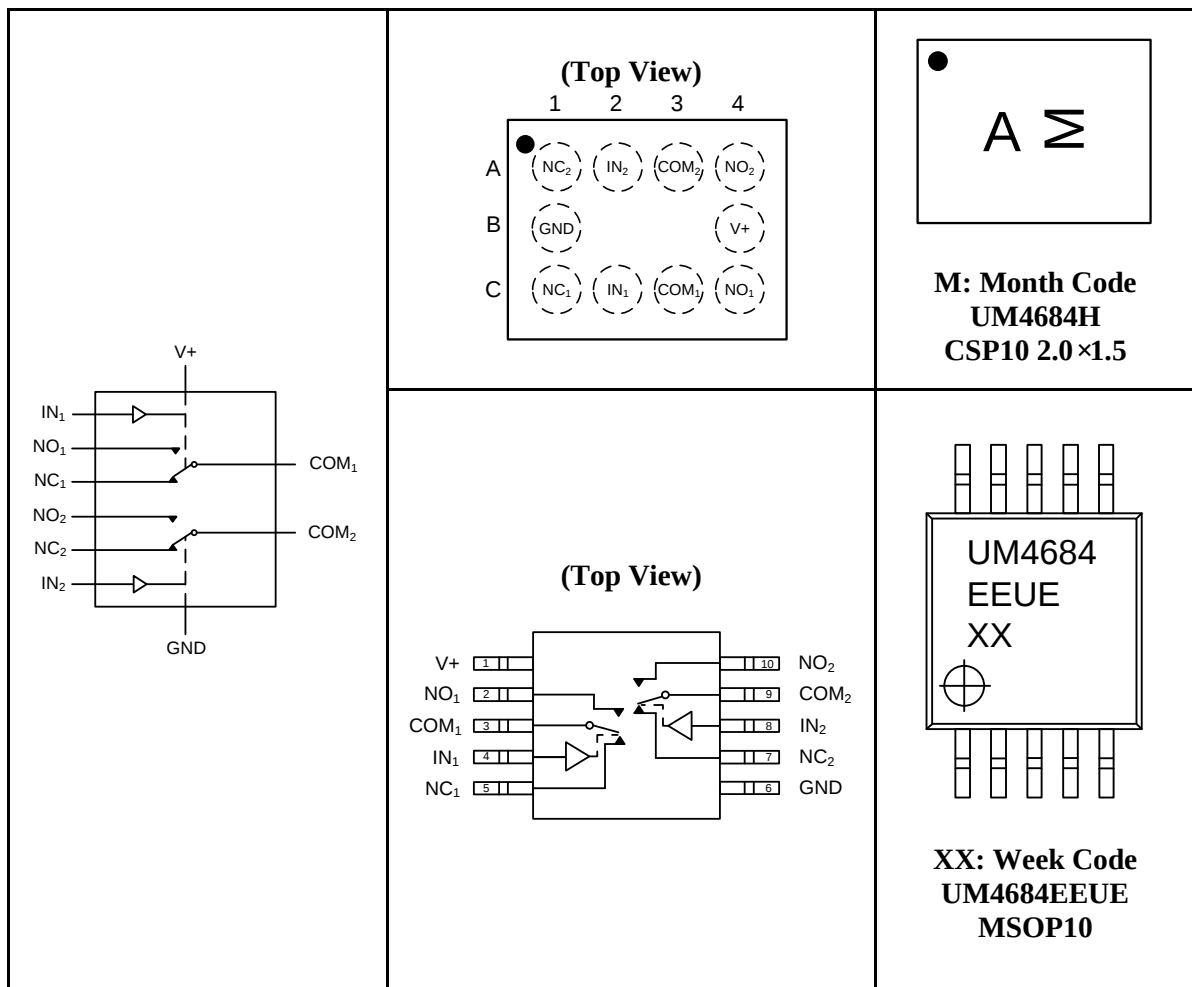
- 手机
- 扬声器耳机切换
- 音频和视频信号路由
- PCMCIA 卡
- 电池供电系统
- 继电器切换
- 电源路由
- 通信电路
- 采用CSP10 & MSOP10封装
- ESD保护>2000V
- +1.8V至+5.5V单电源运行
- NC开关R_{ON}: 0.5Ω (+2.7V电源)
- NO开关R_{ON}: 0.6Ω (+2.7V电源)
- 通道间R_{ON}匹配: 最大0.05Ω (+2.7V电源)
- 信号范围内R_{ON}平坦度: 最大0.2Ω (+2.7V电源)
- 兼容1.8V逻辑电平
- 低串扰: -69dB (100kHz)
- 高隔离度: -69dB (100kHz)

订购信息

芯片型号	温度范围	封装类型	丝印编码	发货信息
UM4684H	-40 ℃ to 85 ℃	CSP10 2.0×1.5	A	3000pcs/7 Inch Tape & Reel
UM4684EEUE	-40 ℃ to 85 ℃	MSOP10	UM4684EEUE	4000pcs/13 Inch Tape & Reel

Pin Configurations

Top View



Ball Mapping for UM4684H

	1	2	3	4
A	NC ₂	IN ₂	COM ₂	NO ₂
B	GND			V+
C	NC ₁	IN ₁	COM ₁	NO ₁

Transparent Top View

Pin Description

Pin Name	Pin Number		Function
	CSP10 2.0×1.5	MSOP10	
NC_	A1, C1	5, 7	Analog Switch—Normally Closed Terminal
IN_	A2, C2	4, 8	Digital Control Input
COM_	A3, C3	3, 9	Analog Switch—Common Terminal
NO_	A4, C4	2, 10	Analog Switch—Normally Open Terminal
V+	B4	1	Positive Supply Voltage Input
GND	B1	6	Ground

Function Table

IN_	NO_	NC_
0	OFF	ON
1	ON	OFF

Absolute Maximum Ratings (Note 1)

Parameter		Value	Unit
Voltage on V+ Pin (Reference to GND)		-0.3 to +6	V
Voltage on IN_, COM_, NC_, NO_ Pins (Note 2) (Reference to GND)		-0.3 to (V ₊ +0.3)	V
Continuous Current (NO_, NC_, COM_)		±300	mA
Peak Current (Pulsed at 1 ms, 10% Duty Cycle)		±500	mA
Storage Temperature		-65 to 150	℃
Package Solder Reflow Conditions (Note 3)	IR/Convection	250	℃
	ESD per Method 3015.7	>2	kV
Power Dissipation (Packages) (Note 4)		CSP10 (Note 5)	457
			mW

Note 1: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Signals on NC_, NO_, or COM_ or IN_ exceeding V₊ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

Note 3: Refer to IPC/JEDEC (J-STD-020B).

Note 4: All bumps welded or soldered to PC Board.

Note 5: Derate 5.7mW/℃ above 70℃.

Electrical Characteristics ($V_+=3V$, $\pm 10\%$ deviation, $V_{IN}=0.5$ or $1.4V$ (Note 6))

Parameter	Symbol	Test Conditions Otherwise Unless Specified	Temp (Note 7)	Limits (-40 °C to 85 °C)			Unit
				Min (Note 9)	Typ (Note 8)	Max (Note 9)	
Analog Switch							
Analog Signal Range (Note 10)	V _{NO} V _{NC} V _{COM}		Full	0		V ₊	V
On-Resistance (Note 10)	R _{on}	V ₊ =2.7V, V _{COM} =0.6/1.5V, I _{NO} , I _{NC} =100mA	Room Full		0.5	0.8 1.0	Ω
R _{ON} Flatness (Note 10)	R _{on} Flatness		Room			0.15	
On-Resistance Match Between Channels (Note 10)	ΔR _{DS(on)}		Room			0.05	
Switch Off Leakage Current	I _{NO(off)} , I _{NC(off)}	V ₊ =3.3V, V _{NO} , V _{NC} =0.3V/3V, V _{COM} =3V/0.3V	Room Full	-2 -20		2 20	nA
	I _{COM(off)}		Room Full	-2 -20		2 20	
Channel-On Leakage Current	I _{COM(on)}	V ₊ =3.3V, V _{NO} , V _{NC} =V _{COM} =0.3V/3V	Room Full	-2 -20		2 20	
Digital Control							
Input High Voltage (Note 10)	V _{INH}		Full	1.4			V
Input Low Voltage	V _{INL}		Full			0.5	
Input Capacitance	C _{IN}		Full		10		pF
Input Current	I _{INL} or I _{INH}	V _{IN} =0 or V ₊	Full	-1		1	μA
Dynamic Characteristics							
Turn-On Time	t _{ON}	V _{NO} or V _{NC} =2.0V, R _L =50Ω, C _L =35pF	Room Full		52	82 90	ns
Turn-Off Time	t _{OFF}		Room Full		43	73 78	
Break-Before-Make Time	t _d	V _{NO} or V _{NC} =2.0V, R _L =50Ω, C _L =35pF	Full	1	6		ns
Charge Injection (Note 10)	Q _{INJ}	C _L =1nF, V _{GEN} =1.5V, R _{GEN} =0Ω	Room		21		pC
Off-Isolation (Note 10)	O _{IRR}	R _L =50Ω, C _L =5pF, f=100kHz	Room		-69		dB
Crosstalk (Note 10)	X _{TALK}		Room		-69		
-3dB Bandwidth	BW	R _L =50Ω, C _L =5pF	Room		20		MHz

NO NC Off Capacitance (Note 10)	$C_{NO(off)}$ $C_{NC(off)}$	$V_{IN}=0$ or V_+ , $f=1MHz$	Room Room		145 145		pF
Channel On Capacitance (Note 10)	$C_{NO(on)}$ $C_{NC(on)}$		Room Room		406 406		
Power Supply							
Power Supply Range	V_+		Full	1.8		5.5	V
Power Supply Current	I_+	$V_{IN}=0$ or V_+	Room Full		0.001	1.0 1.0	μA

Note 6. V_{IN} =input voltage to perform proper function.

Note 7. Room=25 °C, Full=as determined by the operating suffix.

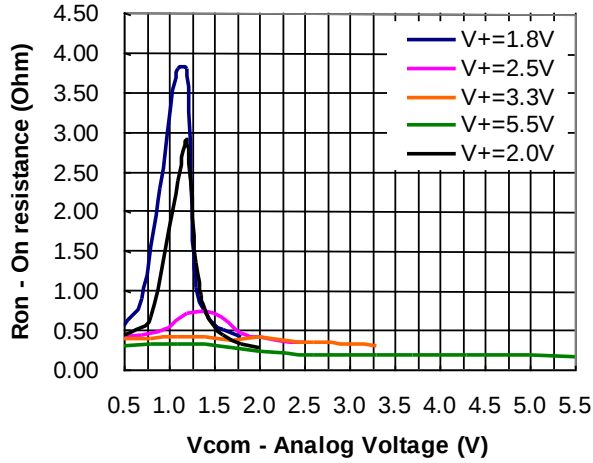
Note 8. Typical values are for design aid only, not guaranteed nor subjected to production testing.

Note 9. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.

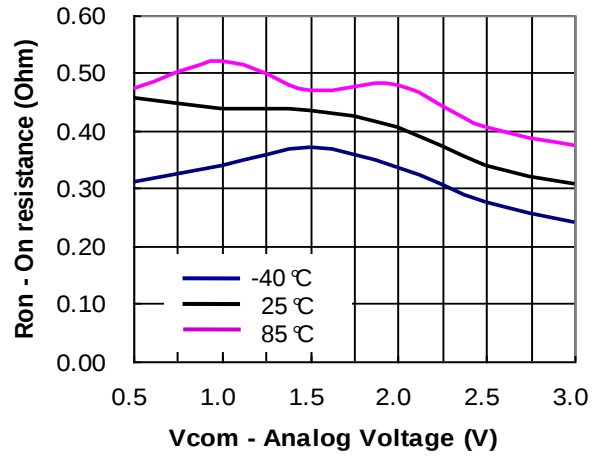
Note 10. Guaranteed by design, nor subjected to production testing.

Typical Operating Characteristics

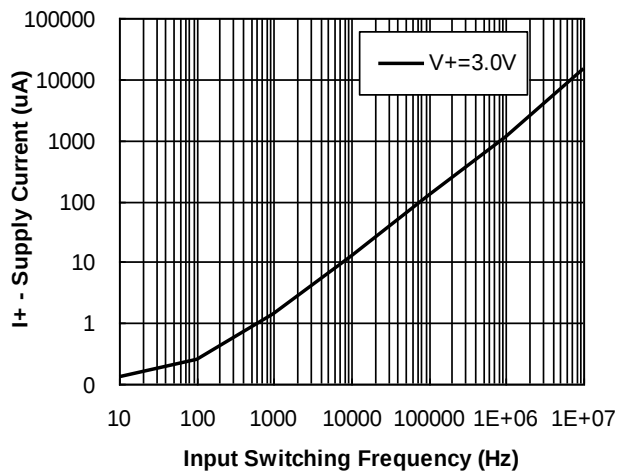
Ron vs.Vcom and Supply Voltage



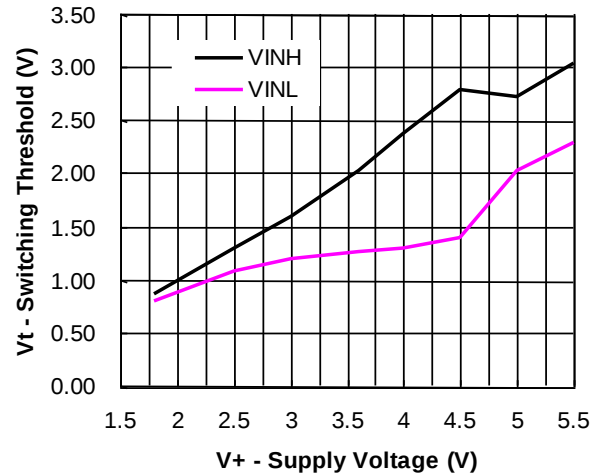
Ron vs.Vcom and Temperature (NC1)



Supply Current vs. Input Switching Frequency

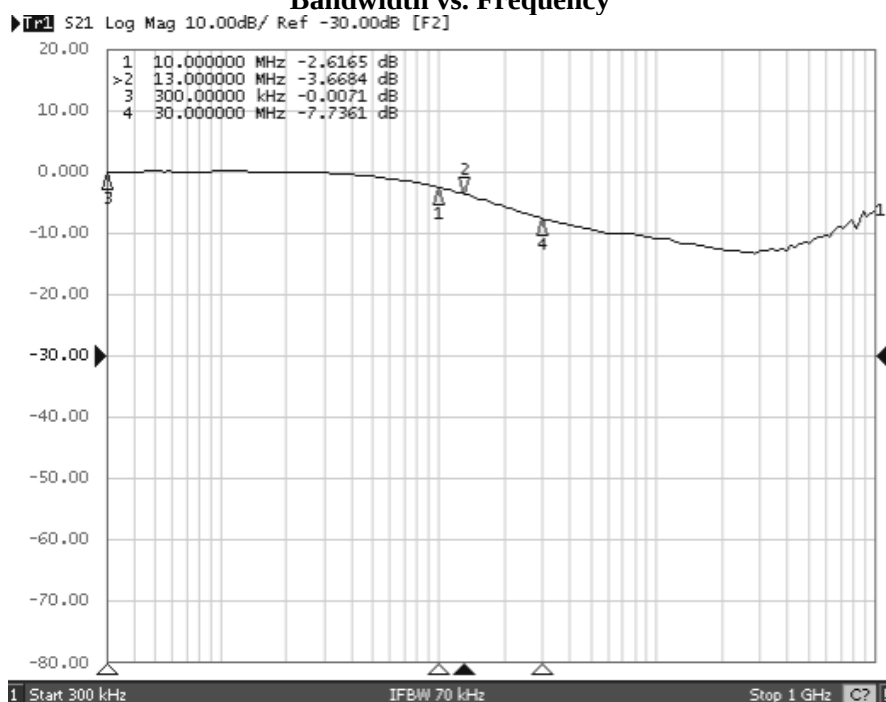


Switching Threshold vs. Supply Voltage (V)

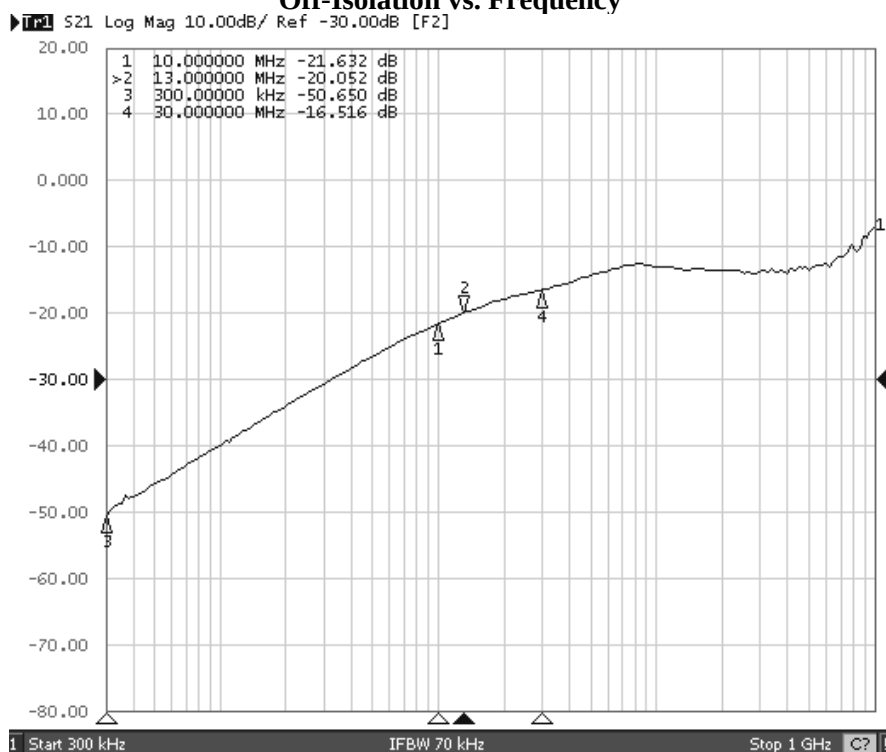


Typical Operating Characteristics (Continued)

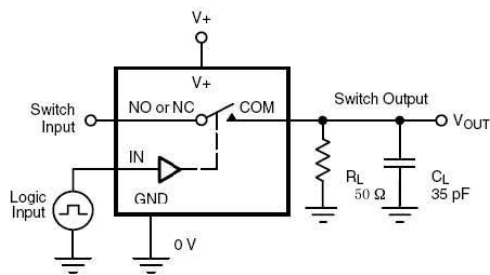
Bandwidth vs. Frequency



Off-Isolation vs. Frequency



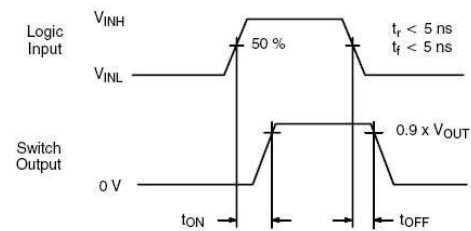
Test Circuits/Timing Diagrams



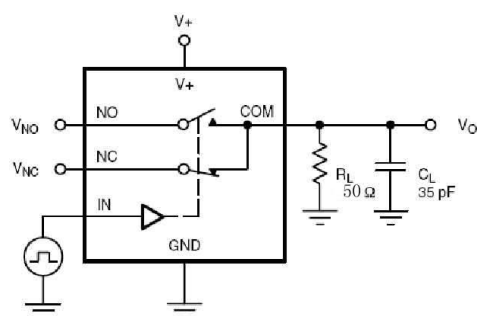
C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM} \left(\frac{R_L}{R_L + R_{ON}} \right)$$

FIGURE 1. Switching Time

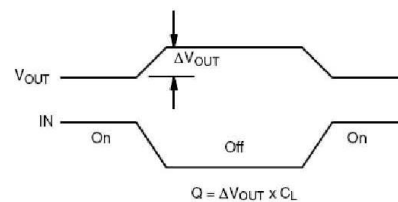
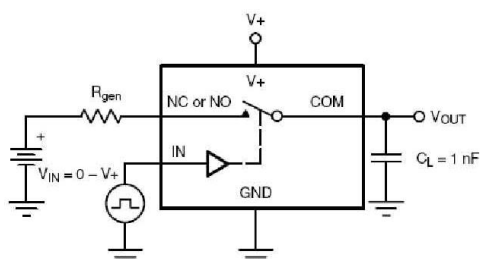
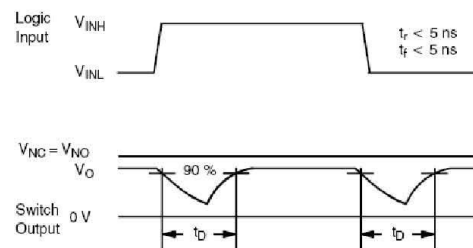


Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.



C_L (includes fixture and stray capacitance)

FIGURE 2. Break-Before-Make Interval



IN depends on switch configuration: input polarity determined by sense of switch.

FIGURE 3. Charge Injection

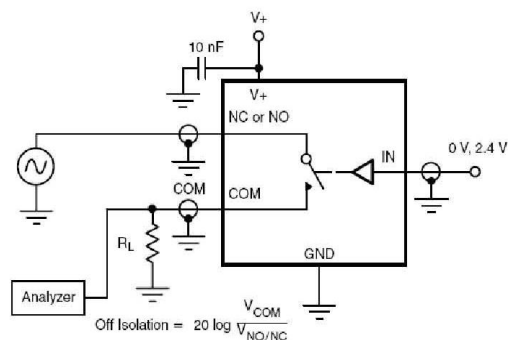


FIGURE 4. Off-Isolation

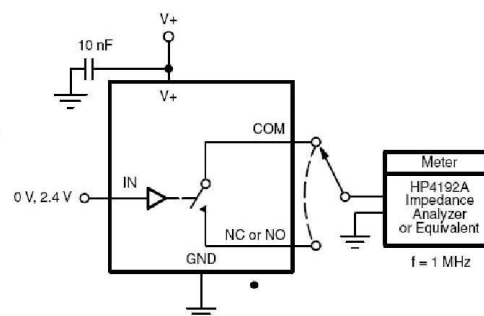


FIGURE 5. Channel Off/On Capacitance

Applications Information

Digital Control Inputs

The UM4684 logic inputs accept up to +5.5V regardless of supply voltage. For example, with a +3.3V supply, IN_ may be driven low to GND and high to 5.5V. Driving IN_ rail-to-rail minimizes power consumption. Logic levels for a +1.8V supply are 0.5V (low) and 1.4V (high).

Analog Signal Levels

Analog signals that range over the entire supply voltage (V_+ to GND) is passed with very little change in on-resistance (see Typical Operating Characteristics). The switches are bidirectional, so the NO_, NC_, and COM_ pins can be either inputs or outputs.

Caution

Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to devices.

Proper power-supply sequencing is recommended for all CMOS devices. Always apply V_+ before applying analog signals, especially if the analog signal is not current limited. If this sequencing is not possible, and if the analog inputs are not current limited to <20mA, add a small signal diode (D1) as shown in Figure 6. Adding a protection diode reduces the analog range to a diode drop (about 0.7V) below V_+ (for D1). RON increases slightly at low supply voltages. Maximum supply voltage (V_+) must not exceed +6V. Protection diode D1 also protects against some over voltage situations. No damage will result on Figure 6's circuit if the supply voltage is below the absolute maximum rating applied to an analog signal pin.

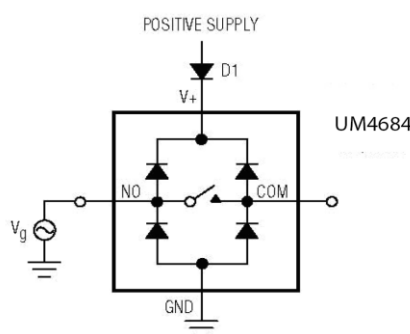


Figure 6

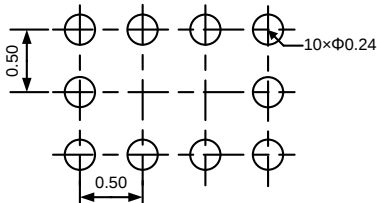
Package Information

UM4684H CSP10 2.0×1.5

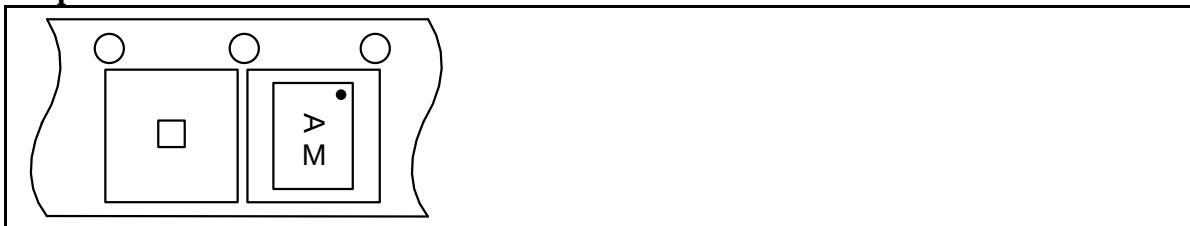
Outline Drawing

DIMENSIONS						
Symbol	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	0.68	0.72	0.76	0.027	0.028	0.030
A1	0.21	0.231	0.24	0.0083	0.0091	0.0094
A2	0.47	0.49	0.52	0.0185	0.0193	0.0205
b	0.27	0.31	0.34	0.011	0.012	0.013
D	2.00	-	2.10	0.079	-	0.083
E	1.50	-	1.60	0.059	-	0.063
e	0.50BSC			0.020BSC		

Land Pattern

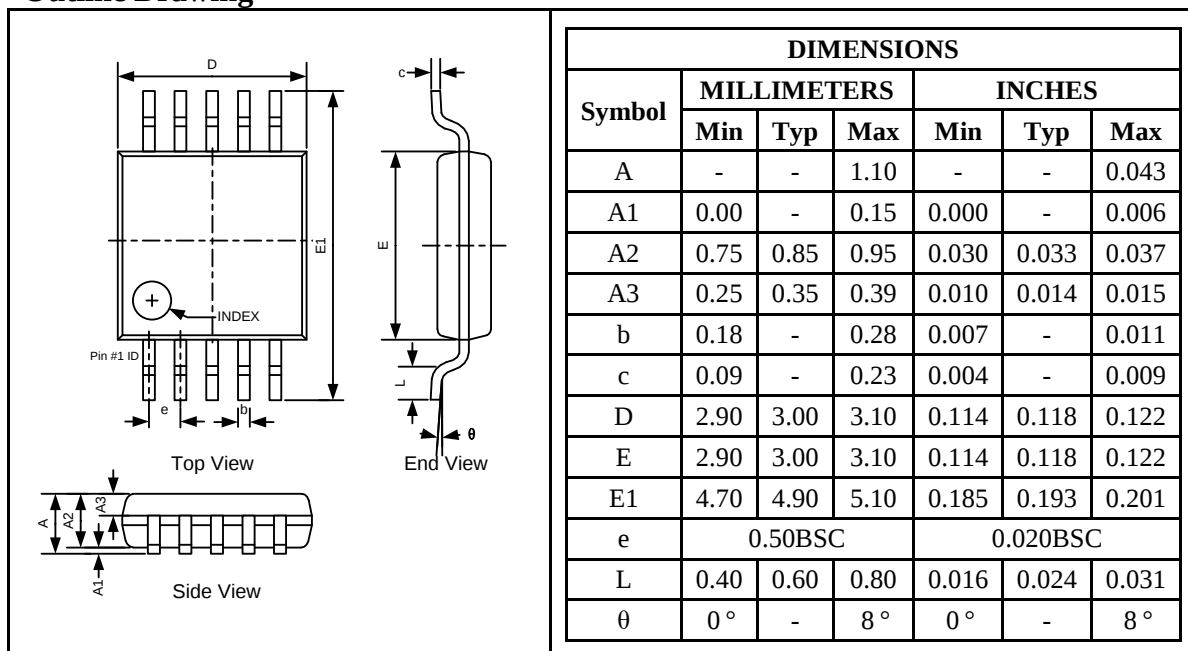
	NOTES: 1. Bump is Lead Free Sn/Ag/Cu; 2. Unit: mm; 3. Non-solder mask defined copper landing pad; 4. Laser Mark on silicon die back; back-lapped.
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Tape and Reel Orientation

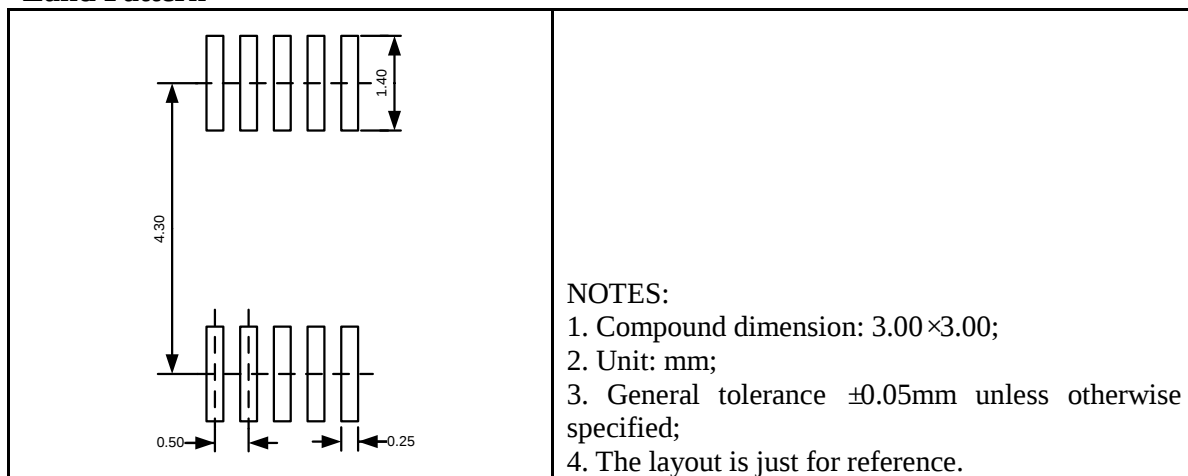


UM4684EEUE MSOP10

Outline Drawing



Land Pattern



Tape and Reel Orientation



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