用于彩色LCD接口的4通道ESD-EMI防护

UM4411 *DFN8 1.7×1.3*

描述

UM4411是一款集成TVS二极管的低通滤波器阵列。该器件专为抑制便携式电子设备中不需要的EMI/RFI信号并提供静电放电 (ESD) 保护而设计。这种先进的器件采用硅雪崩技术，具有卓越的钳位性能和直流电气特性。经过优化，可保护手机及其他便携式电子设备中的彩色液晶显示屏。

UM4411由四路相同的电路组成，每路都集成了用于ESD保护的TVS二极管和用于EMI滤波的RC网络。串联电阻为100Ω，电容为10pF，可在800 MHz至2.5GHz范围内实现25dB的最小衰减。TVS二极管可有效抑制超过±15kV（空气间隙放电）和±8kV（接触放电）的ESD电压，符合IEC 61000-4-2标准的第4级要求。

UM4411采用符合RoHS标准的8引脚DFN8封装。尺寸为1.7mm×1.3mm。引脚间距为0.4mm，表面采用无铅镍钯处理。该封装使其适合用于手机、数码相机和PDA等便携式电子产品。

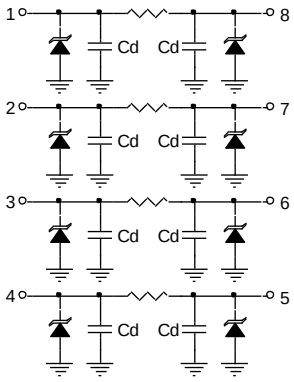
应用

- 数据线的EMI滤波和ESD保护
- 无线电话
- 手持式产品
- 笔记本电脑
- LCD显示器

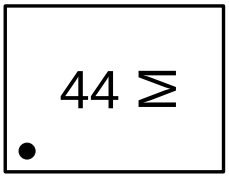
特性

- 集成 TVS 的 EMI/RFI 滤波器，提供静电放电（ESD）保护
- ESD 保护符合 IEC 61000-4-2 第 4 级要求：
  ±15kV（空气间隙放电）
  ±8kV（接触放电）
- 25dB 最小衰减：800MHz 至 2.5GHz
- 工作电压：5V
- 电阻：100Ω ±15%
- 典型电容：10pF (V_R=2.5V)
- 固态硅雪崩技术
- DFN8 封装：1.7mm×1.3 mm
- 湿度敏感等级：1级

引脚配置



顶部视图



M: Month Code
UM4411
DFN8 1.7×1.3

Ordering Information

Part Number	Packaging Type	Marking Code	Shipping Qty
UM4411	DFN8 1.7×1.3	44	3000pcs/7Inch Tape & Reel

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Value	Unit
T_J	Junction Temperature	125	℃
P_R	Steady State Power per Resistor @ 25℃	328	mW
T_{OP}	Operating Temperature Range	-40 to 85	℃
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_L	Maximum Lead Temperature for Soldering	260	℃

Note 1: Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

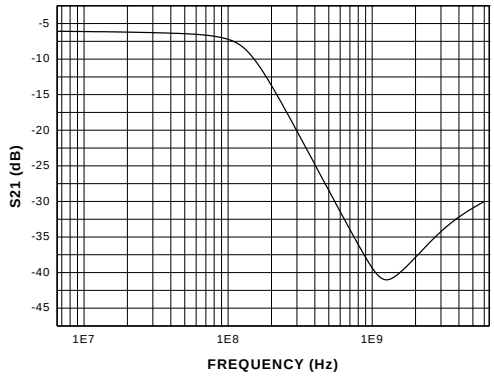
Electrical Characteristics (T_J=25℃ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{RWM}	Reverse Stand-Off Voltage				5.0	V
V_{BR}	Reverse Breakdown Voltage	I_T=1.0mA	6 .0	7.0	8.0	V
I_R	Reverse Leakage Current	V_{RWM}=3.3V			100	nA
R_A	Total Series Resistance	I_R=10mA Each Line	85	100	115	Ω
C_d	Total Capacitance	Input to GND, Each Line V_R=0V, f=1MHz	16	20	24	pF
C_d	Total Capacitance	Input to GND, Each Line V_R=2.5V, f=1MHz	9	10	12	pF
f_{3dB}	Cut-Off Frequency (Note 2)	Above this frequency, appreciable attenuation occurs		150		MHz

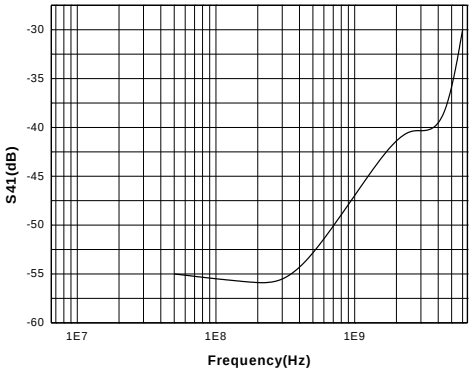
Note 2: 50Ω source and 50Ω load termination.

Typical Operating Characteristics

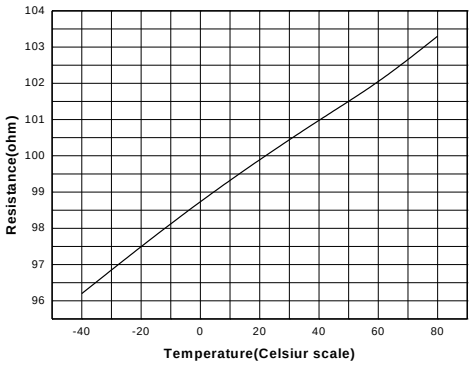
Typical Insertion Loss S21



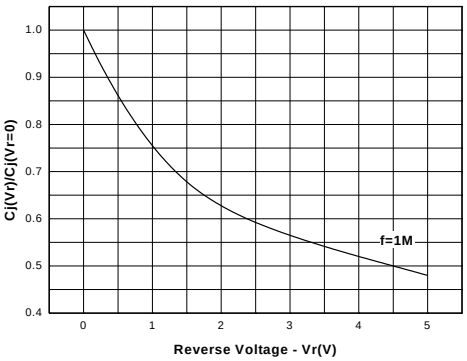
Analog Crosstalk Curve (S41)



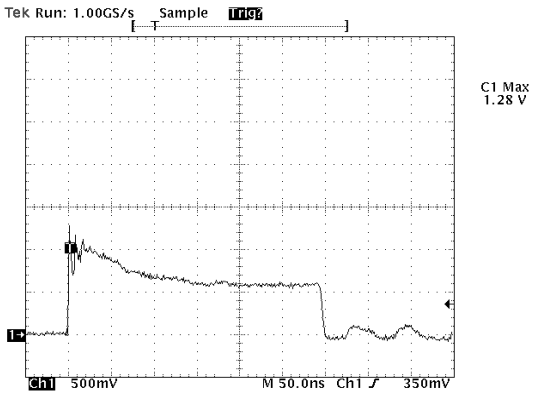
Typical Resistance vs. Temperature



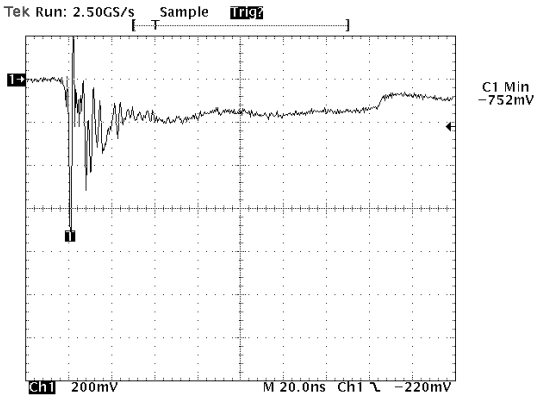
Capacitance vs. Reverse Voltage



ESD Clamping (+8kV Contact)



ESD Clamping (-8kV Contact)



Applications Information

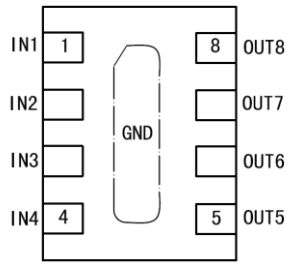
Device Connection

The UM4411 is comprised of four identical circuits each consisting of a low pass filter for EMI/RFI suppression and dual TVS diodes for ESD protection. The device is in an 8-pin DFN package. Electrical connection is made to the 8 pins located at the bottom of the device. A center tab serves as the ground connection. The device has a flow through design for easy layout. Pin connections are noted in Figure 1. All path lengths should be kept as short as possible to minimize the effects of parasitic inductance in the board traces. Recommendations for the ground connection are given below.

Ground Connection Recommendation

Parasitic inductance present in the board layout will affect the filtering performance of the device. As frequency increases, the effect of the inductance becomes more dominant. This effect is given by Equation 1.

Figure 1 - Pin Identification and Configuration
(Top Side View)



Pin	Identification
1 - 4	Input Lines
5 - 8	Output Lines
Center Tab	Ground

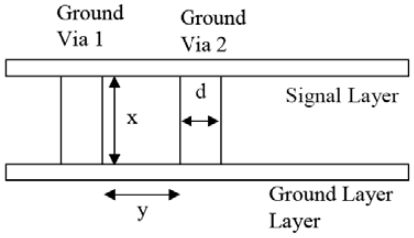
Equation 1: The Impedance of an Inductor at Frequency XLF

$$XLF(L,f) = 2\times\pi\times f\times L$$

Where:
L= Inductance (H)
f = Frequency (Hz)

Via connections to the ground plane form rectangular wire loops or ground loop inductance as shown in Figure 2. Ground loop inductance can be reduced by using multiple vias to make the connection to the ground plane. Bringing the ground plane closer to the signal layer (preferably the next layer) also reduces ground loop inductance. Multiple vias in the device ground pad will result in a lower inductive ground loop over two exterior vias. Vias with a diameter d are separated by a distance y run between layers separated by a distance x. The inductance of the loop path is given by Equation 2. Thus, decreasing distance x and y will reduce the loop inductance and result in better high frequency filter characteristics.

Figure 2 - Inductance of Rectangular Wire Loops



Equation 2: Inductance of Rectangular Wire Loop

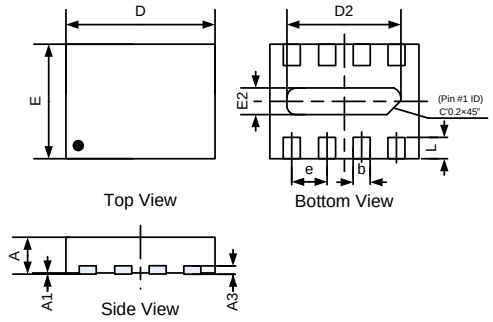
$$LRECT(d,x,y) = 10.16*10^{-9}*\left[x*\ln\left[\frac{2*y}{d}\right]+y*\ln\left[\frac{2*x}{d}\right]\right]$$

Where:
d = Diameter of the wire (in)
x = Length of wire loop (in)
y = Breath of wire loop (in)

Package Information

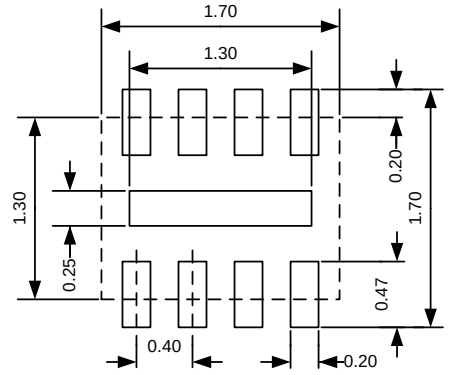
UM4411: DFN8 1.7×1.3

Outline Drawing



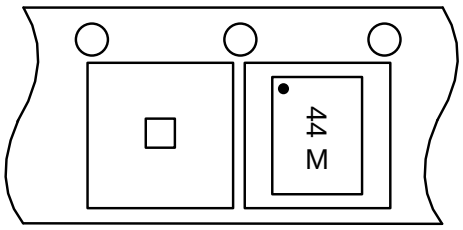
Symbol	DIMENSIONS					
	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	0.45	0.55	0.60	0.018	0.022	0.024
A1	0.00	-	0.05	0.000	-	0.002
A3	0.15REF			0.006REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	1.624	1.70	1.776	0.064	0.067	0.070
D2	0.85	-	1.40	0.033	-	0.055
E	1.25	1.30	1.426	0.049	0.051	0.056
E2	0.20	-	0.50	0.008	-	0.020
e	0.40TYP			0.016TYP		
L	0.17	-	0.37	0.007	-	0.015

Land Pattern



NOTES:
1. Compound dimension: 1.70×1.30;
2. Unit: mm;
3.General tolerance ±0.05mm unless otherwise specified;
4. The layout is just for reference.

Tape and Reel Orientation



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