# *3.3 V 差分多点低电压 M-LVDS 驱动器接收器*

**UM3400S8 *SOP8***
**UM3401S8 *SOP8***

## 描述

UM340XS8系列为纯3.3V电源差分多点低电压（M-LVDS）线路驱动器和接收器。UM3400S8和UM3401S8器件均符合TIA/EIA-899标准。UM3400S8在0.0V下提供1型接收器阈值。UM3401S8在0.1 V下提供2型接收器阈值。

这些器件具有1型和2型接收器，能够在−1V至3.4 V的共模电压范围内，以低至50mV的差分输入电压来检测总线状态。1型接收器具有接近零的阈值(±50 mV)，并具有25mV 的差分输入电压迟滞，以防止在信号缓慢变化或输入丢失时出现输出振荡。2型接收器具有一个偏移阈值，可在开路、闲置总线和其他故障条件下提供可检测电压。UM3400S8和UM3401S8支持单工或半双工总线配置。

## 应用

- 低功耗、高速和短行程可替代TIA/EIA-485
- 背板或电缆连接的多点数据和时钟传输
- 蜂窝基站
- 局端交换机
- 网络交换机和路由器

## 特性

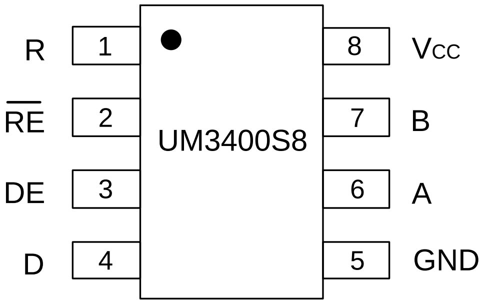
- 低压差分30Ω至55Ω线路驱动器和接收器，信号传输速率高达100Mbps
- 1型接收器具有25mV的迟滞
- 2型接收器具有100mV偏移阈值来检测开路和空闲总线条件
- 符合或超过M-LVDS标准TIA/EIA – 899，适用于多点数据交换
- 可控的驱动器输出电压转换时间，提高信号质量
- –1V至3.4V共模电压范围，允许在2V接地噪声下进行数据传输
- 总线引脚在禁用或$V_{CC} \leq 1.5V$时具有高阻抗
- M-LVDS总线上的无毛刺上电/关断
- Vcc电压范围: $V_{CC}$ = 3.3 ±10% V (3.0 至3.6V)
- 工作环境温度范围：–40 ℃至85 ℃
- 闩锁性能（Latch-up）超过200mA
- 无铅封装

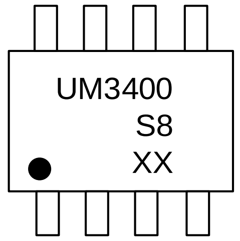
## Ordering Information

| Part Number | Temp. Range | Marking Code | Package Type | Shipping Qty |
|---|---|---|---|---|
| UM3400S8 | -40 ℃ to +85 ℃ | UM3400S8 | SOP8 | 3000pcs/13Inch Tape & Reel |
| UM3401S8 | -40 ℃ to +85 ℃ | UM3401S8 | SOP8 | 3000pcs/13Inch Tape & Reel |

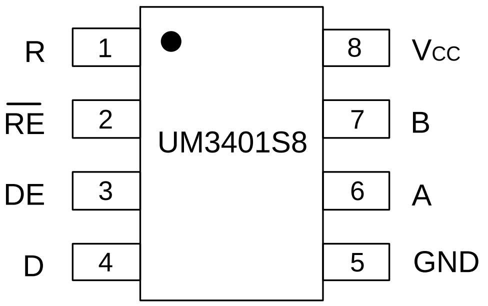
## Pin Configurations

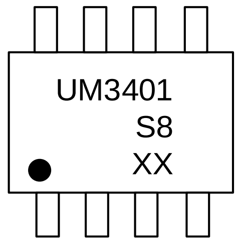
## Top View




**XX: Week Code**
**UM3400S8**
**SOP8**




**XX: Week Code**
**UM3401S8**
**SOP8**

## Pin Description

| Number | Name | I/O Type | Open Default | Function |
|---|---|---|---|---|
| 1 | R | LVCMOS Output | | Receiver Output Pin |
| 2 | $\overline{RE}$ | LVCMOS Input | HIGH | Receiver Enable Input Pin (LOW = Active, HIGH = High Z Output) |
| 3 | DE | LVCMOS Input | LOW | Driver Enable Input Pin (LOW = High Z Output, HIGH=Active) |
| 4 | D | LVCMOS Input | | Driver Input Pin |
| 5 | GND | | | Ground Supply pin. Pin must be connected to power supply to guarantee proper operation. |
| 6 | A | M-LVDS Input/Output | | Transceiver True Input /Output Pin |
| 7 | B | M-LVDS Input/Output | | Transceiver Invert Input /Output Pin |
| 8 | $V_{CC}$ | | | Power Supply pin. Pin must be connected to power supply to guarantee proper operation. |

## Absolute Maximum Ratings（Note1, 2）

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | -0.3 to 4.0 | V |
| $V_{IN}$ | Input Voltage | D, DE,$\overline{RE}$ | -0.3 to 4.0 | V |
| | | A, B (3400, 3401) | -1.8 to 4.0 | |
| $V_{OUT}$ | Output Voltage | R | -0.3 to $V_{CC}$+0.3 | V |
| | | A, B | -1.8 to 4.0 | |
| $T_A$ | Operating Temperature Range, Industrial | | -40 to 85 | ℃ |
| $T_{stg}$ | Storage Temperature Range | | -65 to 150 | ℃ |

Note1: Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Note2: Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and not valid simultaneously. If stress limits are exceeded device functional operation is not implied, damage may occur and reliability may be affected.

## Thermal Characteristics

| Symbol | Thermal Metric | Value | Unit |
|---|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | 110 | ℃/W |
| $\theta_{JC}$ | Junction-to-case thermal resistance | 54 | ℃/W |

## Electrical Characteristics（Static）

$V_{CC}$ = 3.3 ±10% V (3.0 to 3.6V), GND = 0 V, $T_A$ = −40°C to +85°C (See Notes 1, 2, 3)

| Symbol | Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{CC}$ | Power Supply Current | Receiver Disabled and Driver Enabled. $\overline{RE}$ and DE at $V_{CC}$; $R_L$ = 50 Ω; All others open | | 13 | 22 | mA |
| | | Driver and Receiver Disabled. $\overline{RE}$ at $V_{CC}$; DE at 0 V; $R_L$ = No Load; All others open | | 1 | 4 | |
| | | Driver and Receiver Enabled. $\overline{RE}$ at 0 V; DE at $V_{CC}$; $R_L$ = 50 Ω,; All others open | | 16 | 24 | |
| | | Receiver Enabled and Driver Disabled. $\overline{RE}$ at 0v; DE at 0 V; $R_L$ = 50 Ω; All others open | | | 13 | |
| $V_{IH}$ | Input HIGH Voltage | | 2 | | $V_{CC}$ | V |
| $V_{IL}$ | Input LOW Voltage | | GND | | 0.8 | V |
| $V_{BUS}$ | Voltage at any bus terminal $V_A$, $V_B$ | | -1.4 | | 3.8 | V |
| $\|V_{ID}\|$ | Magnitude of differential input voltage | | 0.05 | | $V_{CC}$ | V |
| **Driver** | | | | | | |
| $\|V_{AB}\|$ | Differential output voltage magnitude (see Figure 2) | | 480 | | 650 | mV |
| $\Delta\|V_{AB}\|$ | Change in Differential output voltage magnitude between logic states (see Figure 2) | | -50 | | 50 | mV |
| $V_{OS(SS)}$ | Steady state common mode output voltage (see Figure 3) | | 0.8 | | 1.2 | V |
| $\Delta V_{OS(SS)}$ | Change in Steady state common mode output voltage between logic states (see Figure 3) | | -50 | | 50 | mV |
| $V_{OS(PP)}$ | Peak−to−peak common−mode output voltage (see Figure 3) | | | | 150 | mV |
| $V_{AOC}$ | Maximum steady−state open−circuit output voltage (see Figure 7) | | 0 | | 2.4 | V |
| $V_{BOC}$ | Maximum steady−state open−circuit output voltage (see Figure 7) | | 0 | | 2.4 | V |
| $V_{P(H)}$ | Voltage overshoot, low−to−high level output (see Figure 5) | | | | $1.2V_{SS}$ | V |
| $V_{P(L)}$ | Voltage overshoot, high−to−low level output (see Figure 5) | | $-0.2V_{SS}$ | | | V |
| $I_{IH}$ | High−level input current (D, DE) $V_{IH}$ = 2 V | | 0 | | 10 | μA |
| $I_{IL}$ | Low−level input current (D, DE) $V_{IL}$ = 0.8 V | | 0 | | 10 | μA |
| $\|I_{OS}\|$ | Differential short−circuit output current magnitude (see Figure 4) | | | | 24 | mA |

## Electrical Characteristics（Static）—— continued

$V_{CC}$ = 3.3 ±10%V (3.0 to 3.6V), GND = 0 V, $T_A$ = −40°C to +85°C (See Notes 1，2，3)

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Receiver** | | | | | | |
| $V_{IT+}$ | Positive−going Differential Input voltage Threshold (See Figure 9 & Tables 1 and 2) | Type1 | | | 50 | mV |
| | | Type2 | | | 150 | |
| $V_{IT-}$ | Negative−going Differential Input voltage Threshold (See Figure 9 & Tables 1 and 2) | Type1 | -50 | | | mV |
| | | Type2 | 50 | | | |
| $V_{HYS}$ | Differential Input Voltage Hysteresis (See Figure 9 ) | Type1 | | 25 | | mV |
| | | Type2 | | 0 | | |
| $V_{OH}$ | High−level output voltage ($I_{OH}$ = –8 mA) | | 2.4 | | | V |
| $V_{OL}$ | Low−level output voltage ($I_{OH}$ = 8 mA) | | | | 0.4 | V |
| $I_{IH}$ | $\overline{RE}$ High-level input current ($V_{IH}$ = 2 V) | | -10 | | 0 | μA |
| $I_{IL}$ | $\overline{RE}$ Low-level input current ($V_{IL}$ = 0.8 V) | | -10 | | 0 | μA |
| $I_{OZ}$ | High−impedance state output current ($V_O$ = 0 V or 3.6 V) | | -10 | | 15 | μA |
| $C_A/C_B$ | Input Capacitance $V_I = 0.4\sin(30E^6\pi t) + 0.5$ V, other outputs at 1.2V using HP4194A impedance analyzer (or equivalent) | | | 3 | | pF |
| $C_{AB}$ | Differential Input Capacitance $V_{AB} = 0.4\sin(30E^6\pi t)$ V, other outputs at 1.2 V using HP4194A impedance analyzer (or equivalent) | | | | 2.5 | pF |
| $C_{A/B}$ | Input Capacitance Balance, ($C_A/C_B$) | | 99 | | 101 | % |
| **Bus Input and Output** | | | | | | |
| $I_A$ | Input Current Receiver or Transceiver with Driver Disabled | $V_A$=3.8V, $V_B$=1.2V | 0 | | 32 | μA |
| | | $V_A$=0V or 2.4V, $V_B$=1.2V | -20 | | 20 | |
| | | $V_A$= −1.4V, $V_B$=1.2V | -32 | | 0 | |
| $I_B$ | Input Current Receiver or Transceiver with Driver Disabled | $V_B$=3.8V, $V_A$=1.2V | 0 | | 32 | μA |
| | | $V_B$=0V or 2.4V, $V_A$=1.2V | -20 | | 20 | |
| | | $V_B$= −1.4V, $V_A$=1.2V | -32 | | 0 | |
| $I_{AB}$ | Differential Input Current Receiver or Transceiver with driver disabled ($I_A$−$I_B$) ; $V_A = V_B$ , $−1.4 \le V_A \le 3.8$ V | | -4 | | 4 | μA |
| $I_{A(OFF)}$ | Input Current Receiver or Transceiver Power Off $0V \le V_{CC} \le 1.5$ | $V_A$=3.8V, $V_B$=1.2V | 0 | | 32 | μA |
| | | $V_A$=0V or 2.4V, $V_B$=1.2V | -20 | | 20 | |
| | | $V_A$= −1.4V, $V_B$=1.2V | -32 | | 0 | |
| $I_{B(OFF)}$ | Input Current Receiver or Transceiver Power Off $0V \le V_{CC} \le 1.5$ | $V_B$=3.8V, $V_A$=1.2V | 0 | | 32 | μA |
| | | $V_B$=0V or 2.4V, $V_A$=1.2V | -20 | | 20 | |
| | | $V_B$= −1.4V, $V_A$=1.2V | -32 | | 0 | |
| $I_{AB(OFF)}$ | Receiver Input or Transceiver Input/Output Power Off Differential Input Current; ($I_A$−$I_B$) $V_A = V_B$ , $0 \le V_{CC} \le 1.5$ V, $−1.4 \le V_A \le 3.8$ V | | -4 | | 4 | μA |
| $C_A$ | Transceiver Input Capacitance with Driver Disabled $V_A = 0.4\sin(30E^6\pi t) + 0.5$ V using HP4194A impedance analyzer (or equivalent); $V_B$ = 1.2 V | | | 5 | | pF |
| $C_B$ | Transceiver Input Capacitance with Driver Disabled $V_B = 0.4\sin(30E^6\pi t) + 0.5$ V using HP4194A impedance analyzer (or equivalent); $V_A$ = 1.2 V | | | 5 | | pF |
| $C_{AB}$ | Transceiver Differential Input Capacitance with Driver Disabled $V_A = 0.4\sin(30E^6\pi t) + 0.5$ V using HP4194A impedance analyzer (or equivalent); $V_B$ = 1.2 V | | | | 3.0 | pF |
| $C_{A/B}$ | Transceiver Input Capacitance Balance with Driver Disabled, ($C_A/C_B$) | | 99 | | 101 | % |

## Electrical Characteristics（Static）—— continued

$V_{CC}$ = 3.3 ±10%V (3.0 to 3.6V), GND = 0 V, $T_A$ = −40°C to +85°C (See Notes 1，2，3)

**ESD And Latch Up Performance**

| Symbol | Parameter | | | Value | Unit |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human Body Model (JEDEC Standard 22, Method A114−A) | A, B | ±8 | kV |
| | | | All Other Pins | ±4 | |
| Latch Up Performance | JEDEC Standard No.78D | | | ±200 | mA |

Note1: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

Note2: See Figure 1. DC Measurements reference.

Note3: Typ value at 25 ℃ and 3.3V $V_{CC}$ supply voltage

## Electrical Characteristics（Dynamic）

$V_{CC}$ = 3.3 ±10% V (3.0 to 3.6 V), GND = 0 V, $T_A$ = −40°C to +85°C (Note 1,2)

| Symbol | Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Driver** | | | | | | |
| $t_{PLH}/t_{PHL}$ | Propagation Delay (See Figure 5) | | 2.0 | 2.5 | 3.5 | ns |
| $t_{PHZ}/t_{PLZ}$ | Disable Time HIGH or LOW state to High Impedance (See Figure 6) | | | | 7 | ns |
| $t_{PZH}/t_{PZL}$ | Enable Time High Impedance to HIGH or LOW state (See Figure 6) | | | | 7 | ns |
| $t_{SK(P)}$ | Pulse Skew ($\lvert t_{PLH} - t_{PHL}\rvert$) (See Figure 5) | | | | 350 | ps |
| $t_{SK(PP)}$ | Device to Device Skew similar path and conditions (See Figure 5) | | | | 0.9 | ns |
| $t_{JIT(PER)}$ | Period Jitter RMS, 50 MHz (Source $t_r/t_f$ 0.5 ns, 10 and 90 % points, 30k samples. Source jitter de−embedded from Output values) (See Figure 8) | | | 2 | 3 | ps |
| $t_{JIT(PP)}$ | Peak−to−peak Jitter, 100 Mbps $2^{15}$-1 PRBS (Source $t_r/t_f$ 0.5 ns, 10 and 90% points, 100k samples. Source jitter de−embedded from Output values) (See Figure 8) | | | 30 | 130 | ps |
| $t_r/t_f$ | Differential Output rise and fall times (See Figure 5) | | 0.5 | | 1 | ns |
| **Receiver** | | | | | | |
| $t_{PLH}/t_{PHL}$ | Propagation Delay (See Figure 10) | | 2 | 3.6 | 6 | ns |
| $t_{PHZ}/t_{PLZ}$ | Disable Time HIGH or LOW state to High Impedance (See Figure 11) | | | | 10 | ns |
| $t_{PZH}/t_{PZL}$ | Enable Time High Impedance to HIGH or LOW state (See Figure 11) | | | | 15 | ns |
| $t_{SK(P)}$ | Pulse Skew ($\lvert t_{PLH} - t_{PHL}\rvert$) (See Figure 10), $C_L$=15pF | Type1 | | 100 | 300 | ps |
| | | Type2 | | 500 | 850 | |
| $t_{SK(PP)}$ | Device to Device Skew similar path and conditions (See Figure 10) $C_L$=15pF | | | | 1 | ns |
| $t_{JIT(PER)}$ | Period Jitter RMS, 50 MHz (Source: VID = 200 $mV_{PP}$ f $V_{CM}$ =1 V, $t_r/t_f$ 0.5 ns, 10 and 90 % points, 30k samples. Source jitter de−embedded from Output values ) (See Figure 12) | | | 4 | 7 | ps |
| $t_{JIT(PP)}$ | Peak−to−peak Jitter, 100 Mbps $2^{15}$-1 PRBS (Source $t_r/t_f$ 0.5 ns, 10 and 90% points, 100k samples. Source jitter de−embedded from Output values) (See Figure 12) | Type1 | | 200 | 700 | ps |
| | | Type2 | | 225 | 800 | |
| $t_r/t_f$ | Differential Output rise and fall times (See Figure 12), $C_L$=15pF | | 2.3 | | 3.5 | ns |

Note1: Device will meet the specifications after thermal equilibrium has been established when

mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

Note2: Typ value at 25 ℃ and 3.3 $V_{CC}$ supply voltage.

## Parameter Measurement Information

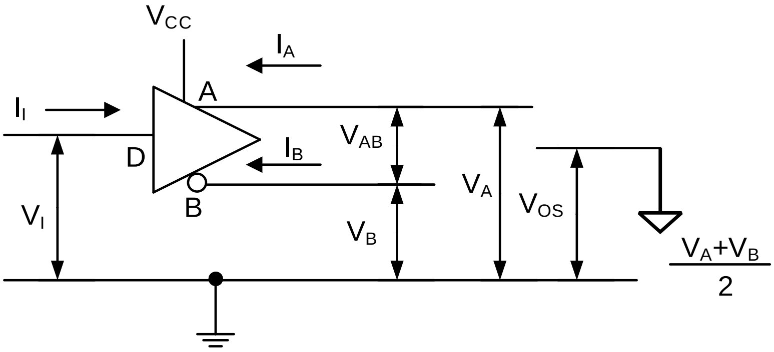
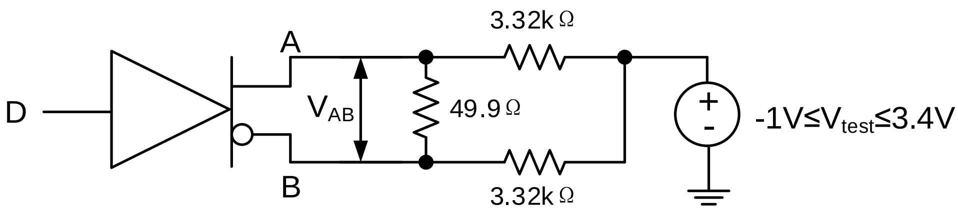
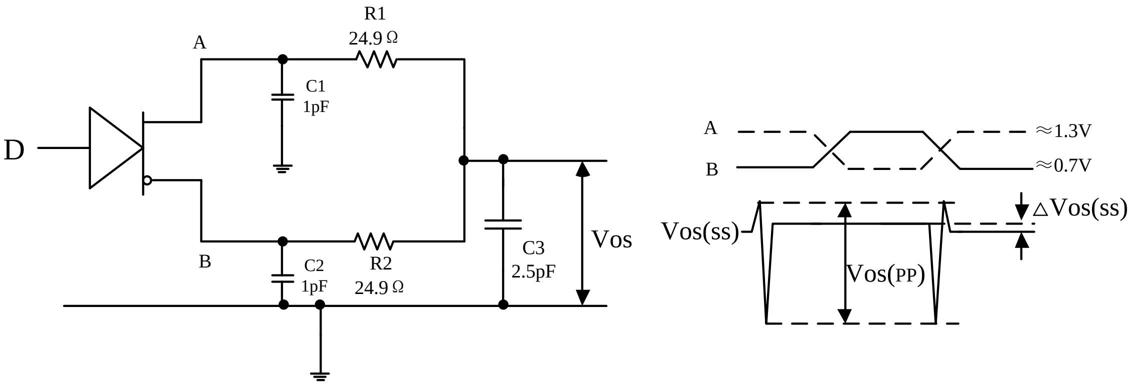



**Figure 1. Driver Voltage and Current Definitions**




Notes: A. All resistors are 1% tolerance.

**Figure 2. Differential Output Voltage Test Circuit**




Notes: A. All input pulses are supplied by a generator having the following characteristics: $t_r$ or $t_f \le 1ns$, pulse frequency = 500 kHz, duty cycle = 50 ±5%.

B. C1, C2 and C3 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are 20% tolerance.

C. R1 and R2 are metal film, surface mount, 1% tolerance, and located within 2 cm of the D.U.T.

D. The measurement of $V_{OS(PP)}$ is made on test equipment with a –3 dB bandwidth of at least 1 GHz.

**Figure 3. Test Circuit and Definitions for the Driver Common−Mode Output Voltage**

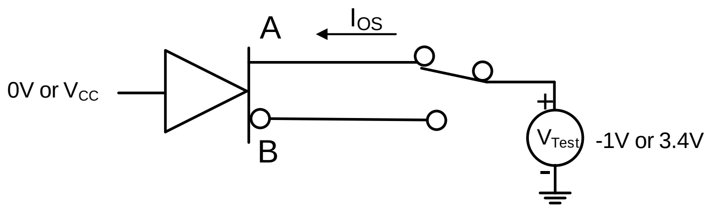
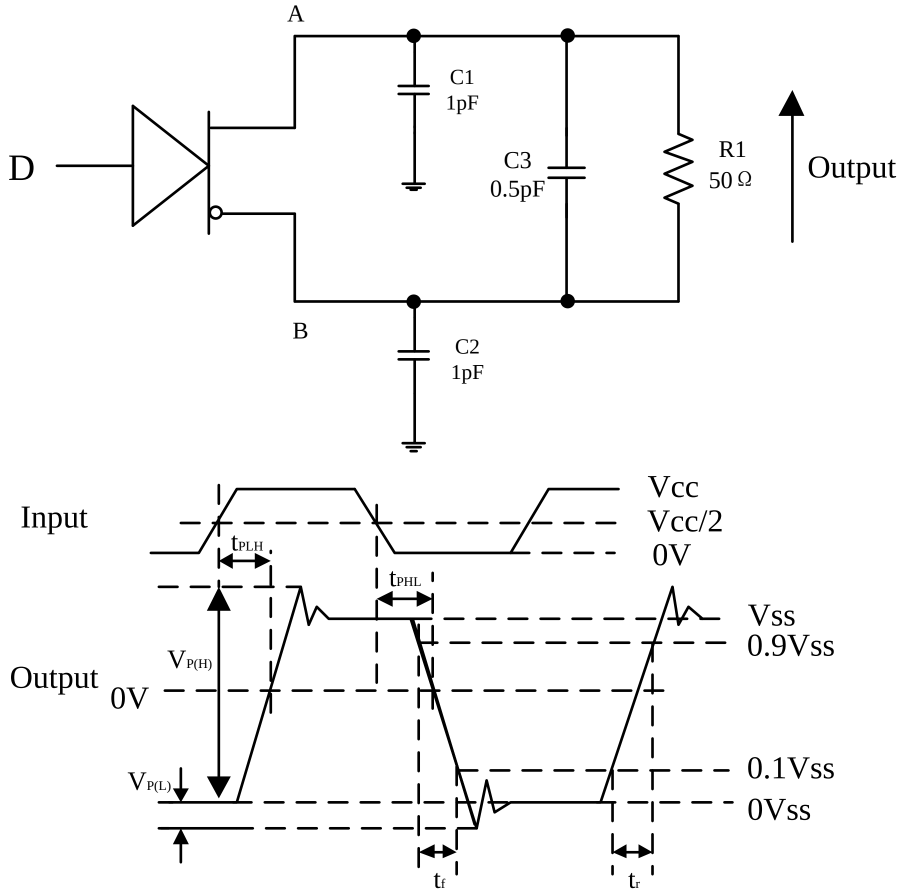



**Figure 4. Driver Short−Circuit Test Circuit**



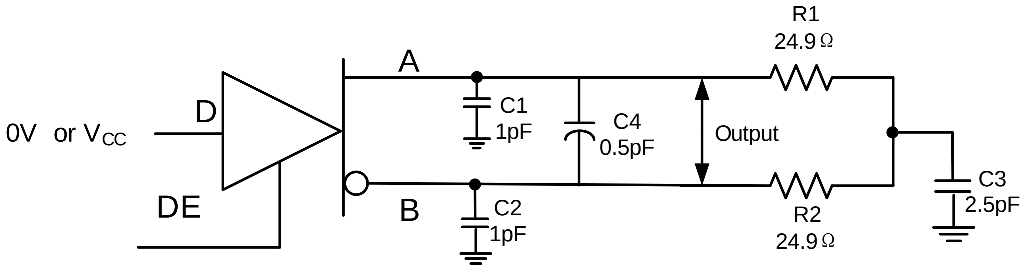

Notes: A. All input pulses are supplied by a generator having the following characteristics: $t_r$ or $t_f \leq$ 1ns, frequency = 500 kHz, duty cycle = 50 ±5%.

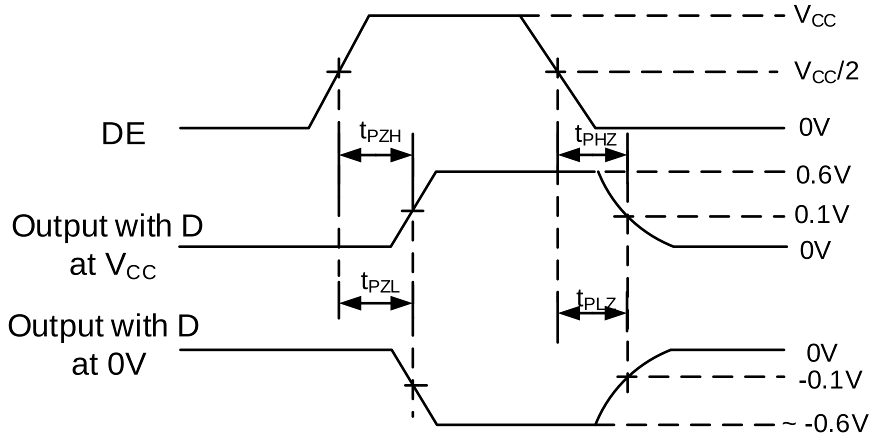
B. C1, C2 and C3 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are 20%.

C. R1 is a metal film, surface mount, and 1% tolerance and located within 2 cm of the D.U.T.

D. The measurement is made on test equipment with a –3 dB bandwidth of at least 1 GHz.

**Figure 5. Driver Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal**




Notes: A. All input pulses are supplied by a generator having the following characteristics: $t_r$ or $t_f \leq$ 1ns, frequency = 500 kHz, duty cycle = 50 ±5%.

B. C1, C2 and C3 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are 20%.

C. R1 and R2 are metal film, surface mount, and 1% tolerance and located within 2 cm of the D.U.T.

D. The measurement is made on test equipment with a –3 dB bandwidth of at least 1 GHz.

**Figure 6. Driver Enable and Disable Time Circuit and Definitions**

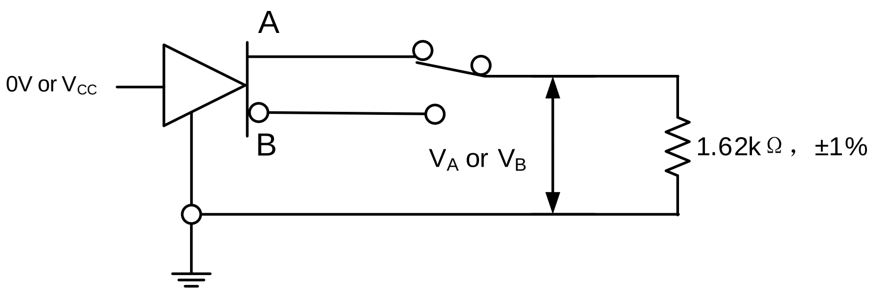
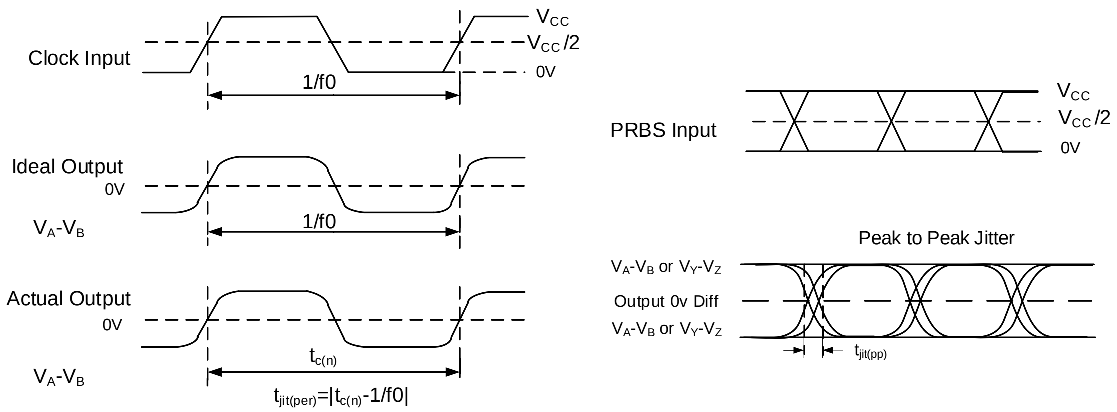



**Figure 7. Maximum Steady State Output Voltage**




Notes: A. All input pulses are supplied by an Agilent 8304A Stimulus System.
B. The measurement is made on a TEK TDS6604 running TDSJIT3 application software
C. Period jitter is measured using a 50 MHz 50 ±1% duty cycle clock input.
D. Peak–to–peak jitter is measured using a 100 Mbps $2^{15}$–1 PRBS input.

**Figure 8. Driver Jitter Measurement Waveforms**

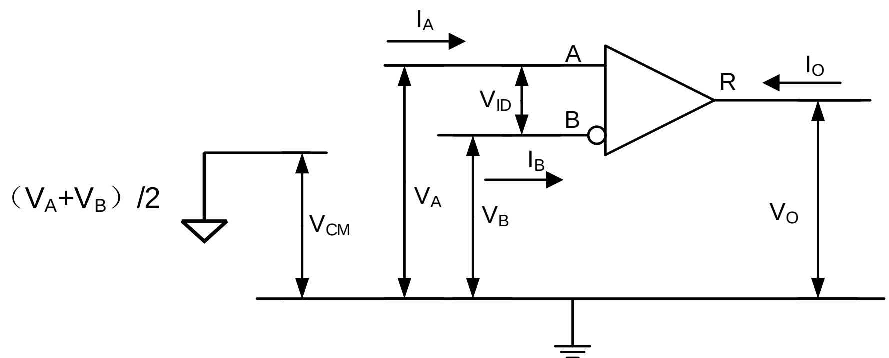
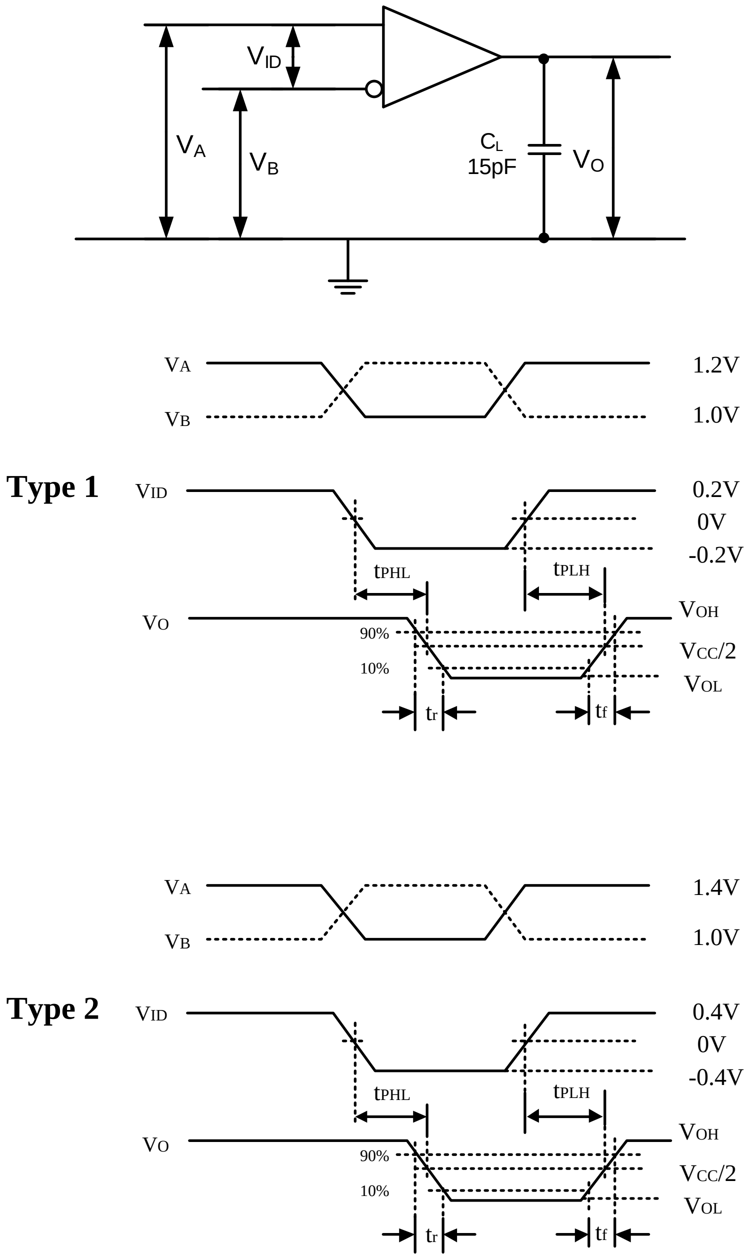
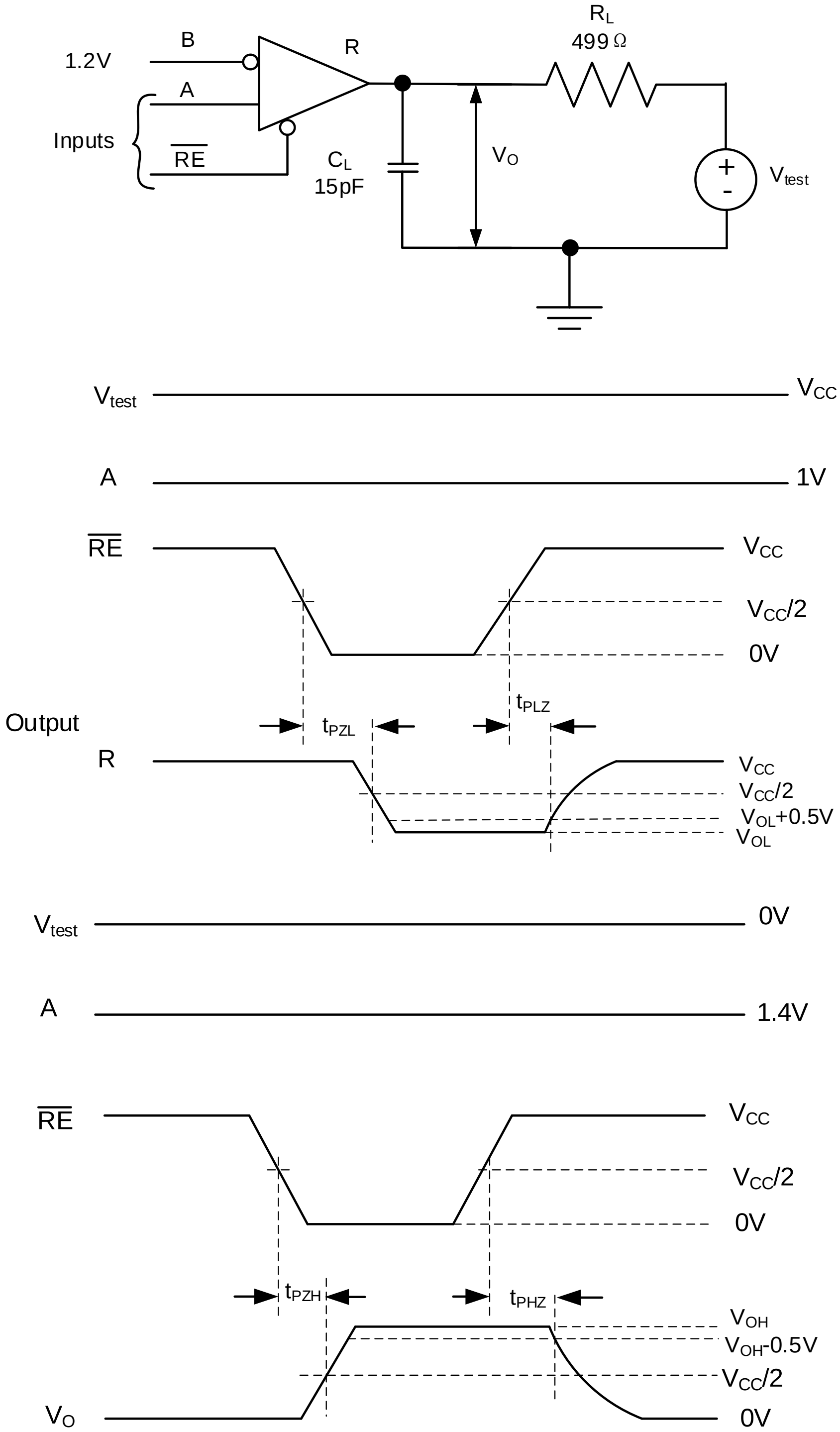



**Figure 9. Receiver Voltage and Current Definitions**



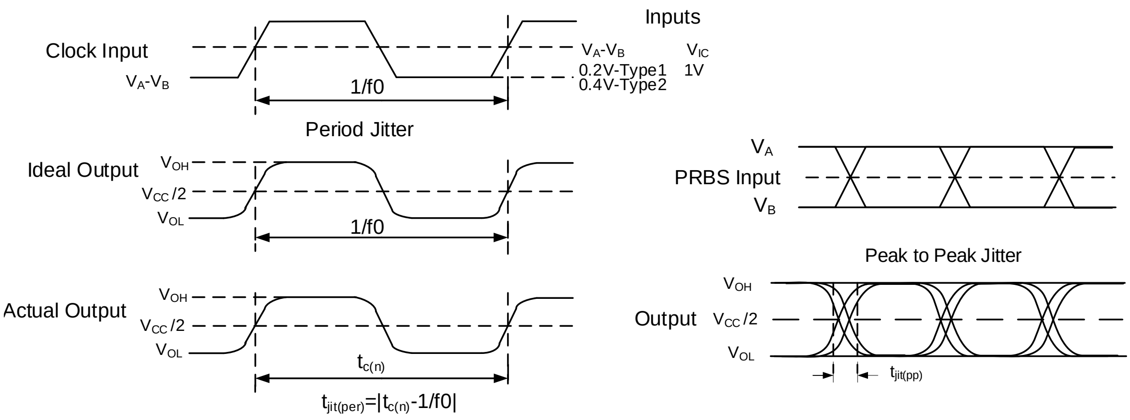

Notes： A. All input pulses are supplied by a generator having the following characteristics:
tr or tf ≤ 1 ns, frequency = 1 MHz, duty cycle = 50±5%. $C_L$ is a combination of a 20%−tolerance, low−loss ceramic, surface−mount capacitor and fixture capacitance within 2 cm of the D.U.T.
B. The measurement is made on test equipment with a –3 dB bandwidth of at least 1 GHz.

**Figure 10. Receiver Timing Test Circuit and Waveforms**




Notes： A. All input pulses are supplied by a generator having the following characteristics:
$t_r$ or $t_f \leq 1$ ns, frequency = 500 kHz, duty cycle = 50±5%.
B. $R_L$ is 1% tolerance, metal film, surface mount, and located within 2 cm of the D.U.T.
C. $C_L$ is the instrumentation and fixture capacitance within 2 cm of the DUT and 20%.

**Figure 11. Receiver Enable/Disable Time Test Circuit and Waveforms**




Notes: A. All input pulses are supplied by an Agilent 8304A Stimulus System.
B. The measurement is made on a TEK TDS6604 running TDSJIT3 application software
C. Period jitter is measured using a 50 MHz 50 ±1% duty cycle clock input.
D. Peak−to−peak jitter is measured using a 100 Mbps $2^{15}-1$ PRBS input.

**Figure 12. Receiver Jitter Measurement Waveforms**

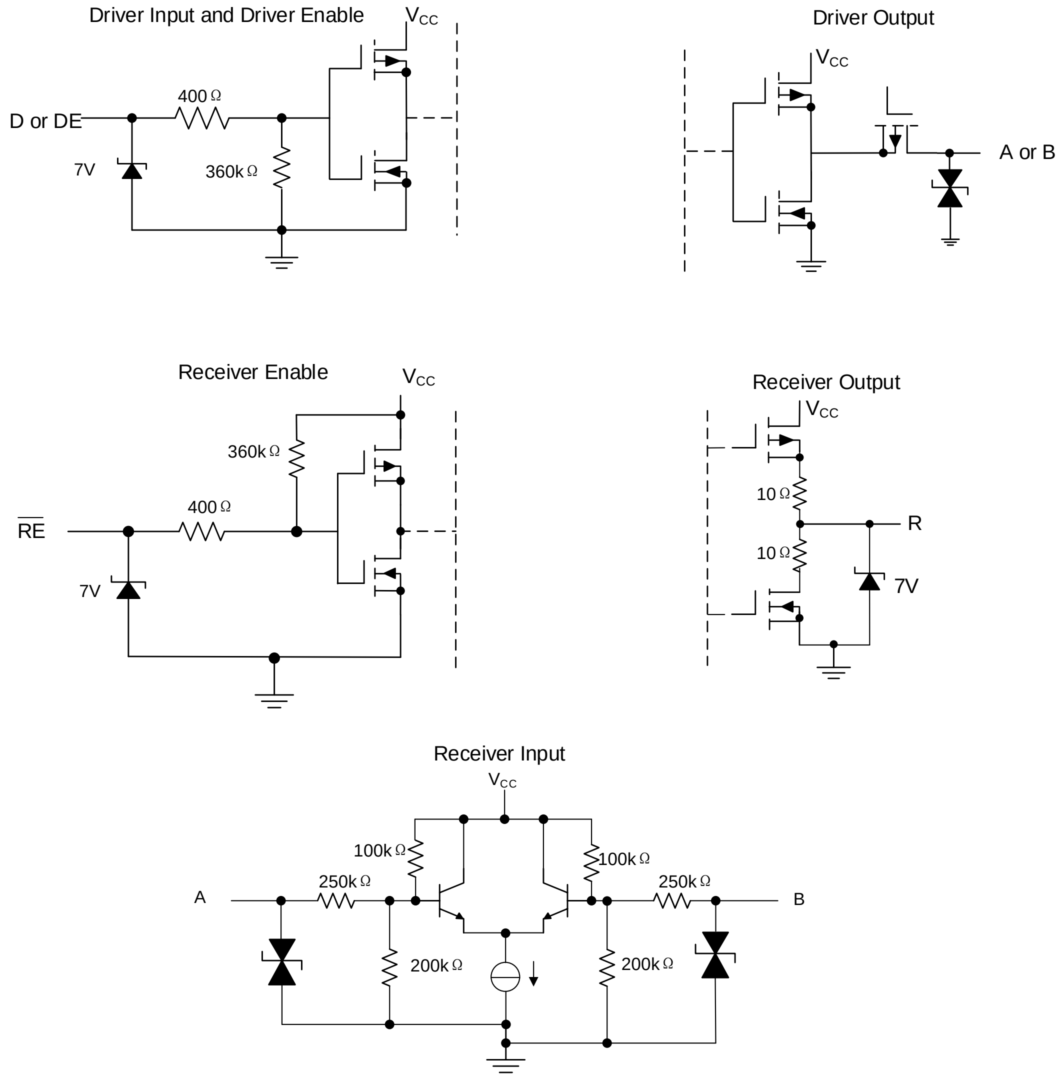



**Figure 13. Equivalent Input and Output Schematic Diagrams**

**Table 1. Type1 Receiver Input Threshold Test Voltages**

| **Applied Voltages** | | **Resulting Differential Input Voltage** | **Resulting Common−Mode Input Voltage** | **Receiver Output (Note1)** |
|---|---|---|---|---|
| **$V_{IA}$** | **$V_{IB}$** | **$V_{ID}$** | **$V_{IC}$** | |
| 2.400 | 0.000 | 2.400 | 1.200 | H |
| 0.000 | 2.400 | –2.400 | 1.200 | L |
| 3.425 | 3.375 | 0.050 | 3.400 | H |
| 3.375 | 3.425 | –0.050 | 3.400 | L |
| -0.975 | -1.025 | 0.050 | –1.000 | H |
| -1.025 | -0.975 | –0.050 | –1.000 | L |

Note1: H = High level, L = Low level, output state assumes receiver is enabled ($\overline{RE}$=L)

Table 2. Type2 Receiver Input Threshold Test Voltage

| Applied Voltages | | Resulting Differential Input Voltage | Resulting Common−Mode Input Voltage | Receiver Output (Note ) |
|---|---|---|---|---|
| $V_{IA}$ | $V_{IB}$ | $V_{ID}$ | $V_{IC}$ | |
| 2.400 | 0.000 | 2.400 | 1.200 | H |
| 0.000 | 2.400 | –2.400 | 1.200 | L |
| 3.475 | 3.325 | 0.150 | 3.400 | H |
| 3.425 | 3.375 | 0.050 | 3.400 | L |
| -0.925 | -1.075 | 0.150 | –1.000 | H |
| -0.975 | -1.025 | 0.050 | –1.000 | L |

Note: H = High level, L = Low level, output state assumes receiver is enabled ($\overline{RE}$=L)

## Device function

Table 3. Device function Table

| | Inputs | | Output | |
|---|---|---|---|---|
| **Type 1 Receiver (UM3400)** | $V_{ID} = V_A - V_B$ | $\overline{RE}$ | R | |
| | $V_{ID} \geq 50$ mV | L | H | |
| | $-50$ mV $< V_{ID} < 50$ mV | L | ? | |
| | $V_{ID} \leq -50$ mV | L | L | |
| | X | H | Z | |
| | X | Open | Z | |
| | Open | L | ? | |
| **Type 2 Receiver (UM3401)** | **Inputs** | | **Output** | |
| | $V_{ID} = V_A - V_B$ | $\overline{RE}$ | R | |
| | $V_{ID} \geq 150$ mV | L | H | |
| | 50 mV $< V_{ID} < 150$ mV | L | ? | |
| | $V_{ID} \leq 50$ mV | L | L | |
| | X | H | Z | |
| | X | Open | Z | |
| | Open | L | L | |
| **Driver** | **Input** | **Enable** | **Output** | |
| | D | DE | A / Y | B / Z |
| | L | H | L | H |
| | H | H | H | L |
| | Open | H | L | H |
| | X | Open | Z | Z |
| | X | L | Z | Z |

H = High, L = Low, Z = High Impedance, X = Don’t Care, ? = Indeterminate

## Applications Information

### Receiver Input Threshold (Failsafe)

The MLVDS standard defines a type 1 and type 2 receiver. Type 1 receivers include no provisions for failsafe and have their differential input voltage thresholds near zero volts.Type 2 receivers have their differential input voltage thresholds offset from zero volts to detect the absence of a voltage difference. The impact to receiver output by the offset input can be seen in Table 3 and Figure 14.

**Table 3. Receiver Input Threshold Requirements**

| Receiver Type | Output Low | Output High |
|---|---|---|
| **Type 1** | $-2.4\text{ V} \le V_{ID} \le -0.05\text{ V}$ | $0.05\text{ V} \le V_{ID} \le 2.4\text{ V}$ |
| **Type 2** | $-2.4\text{ V} \le V_{ID} \le 0.05\text{ V}$ | $0.15\text{ V} \le V_{ID} \le 2.4\text{ V}$ |

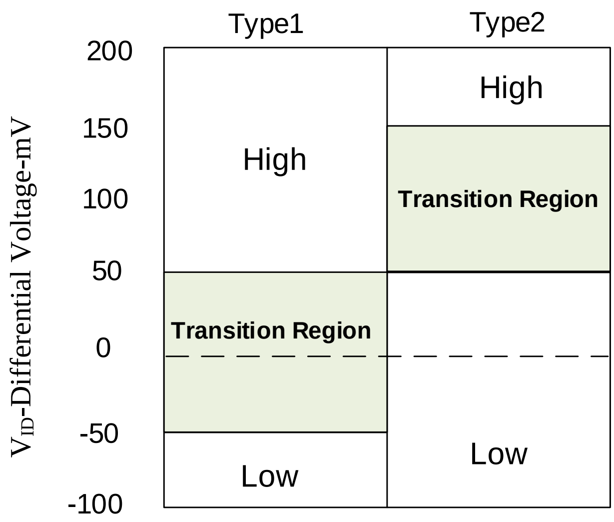



**Figure 14. Receiver Differential Input Voltage Showing Transition Regions by Type**

### Live Insertion/Glitch−Free Power Up/Down

The UM3400/3401 provides a glitch−free power up/down feature that prevents the M−LVDS outputs of the device from turning on during a power up or power down event. This is especially important in live insertion applications, when a device is physically connected to an M−LVDS multipoint bus and $V_{CC}$ is ramping. While the M−LVDS interface for these devices is glitch free on power up/down, the receiver output structure is not. The glitch on the R pin is independent of the RE voltage. Any complications or issues from this glitch are easily resolved in power sequencing or system requirements that suspend operation until $V_{CC}$ has reached a steady state value.

**Simplex Theory Configurations:** Data flow is unidirectional and Point−to−Point from one Driver to one Receiver. UM3400 and UM3401 devices provide a high signal current allowing long drive runs and high noise immunity. Single terminated interconnects yield high amplitude levels. Parallel terminated interconnects yield typical MLVDS amplitude levels and minimizes reflections. See Figures 15 and 16. A UM3400 and UM3401 can be used as the driver or as a receiver.

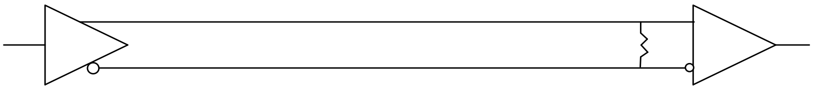


**Figure 15. Point−to−Point Simplex Single Termination**

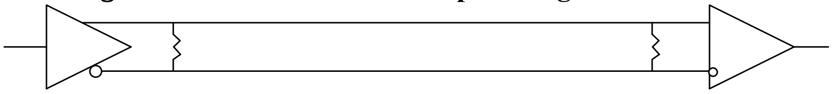


**Figure 16. Parallel−Terminated Simplex**

**Simplex Multidrop Theory Configurations**: Data flow is unidirectional from one Driver with one or more Receivers Multiple boards required. Single terminated interconnects yield high amplitude levels. Parallel terminated interconnects yield typical MLVDS amplitude levels and minimizes reflections. On the Evaluation Test Board, Headers P1, P2, and P3 may be used as need to interconnect transceivers to a each other or a bus. See Figures 20 and 21. A UM3400 and UM3401 can be used as the driver or as a receiver.

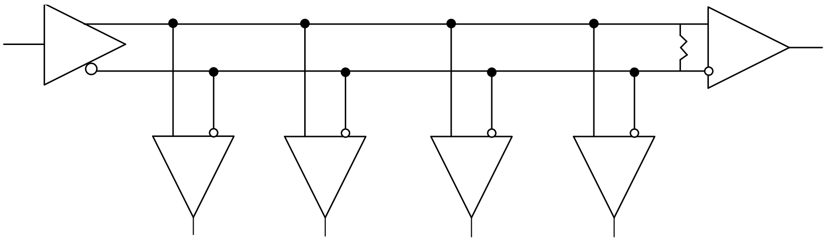


**Figure 17. Multidrop or Distributed Simplex with Single Termination**

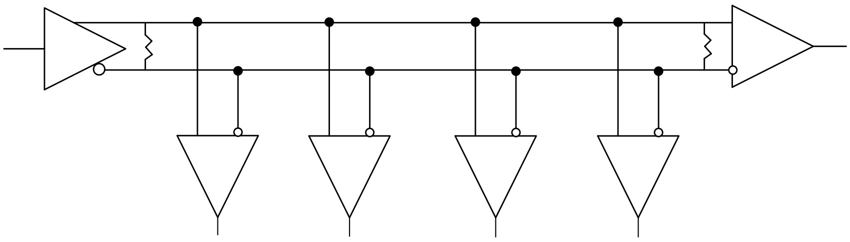


**Figure 18. Multidrop or Distributed Simplex with Double Termination**

**Half Duplex Multinode Multipoint Theory Configurations:** Data flow is unidirectional and selected from one of multiple possible Drivers to multiple Receivers. One “Two Node” multipoint connection can be accomplished with a single evaluation test board. More than Two Nodes requires multiple evaluation test boards. Parallel terminated interconnects yield typical MLVDS amplitude levels and minimizes reflections. Parallel terminated interconnects yield typical LMVDS amplitude levels and minimizes reflections. On the Test Board, Headers P1, P2, and P3 may be used as need to interconnect transceivers to each other or a bus. See Figure 19. A UM3401 can be used as the driver or as a receiver.

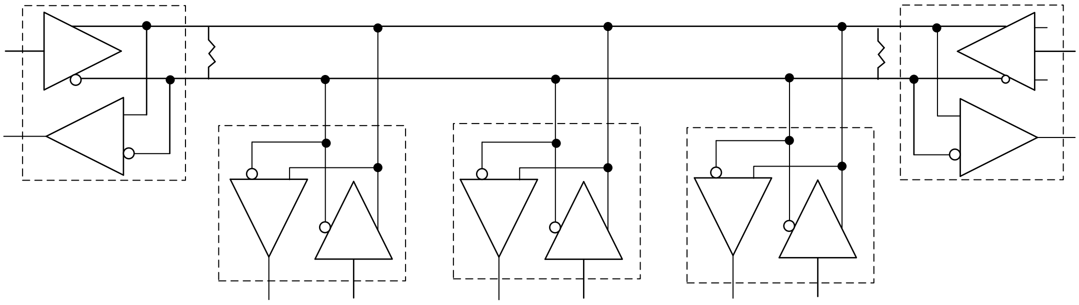
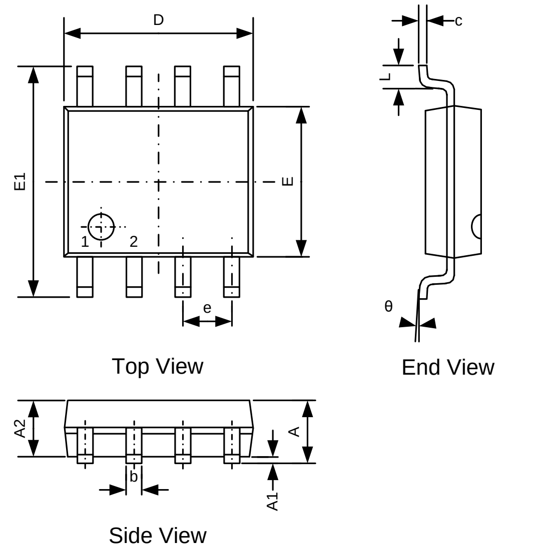


**Figure 19. Multinode Multipoint Half Duplex (Requires Double Termination)**

## Package Information

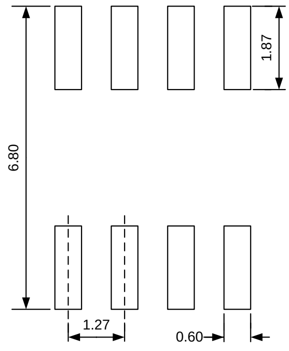
### UM3400 SOP8

**Outline Drawing**



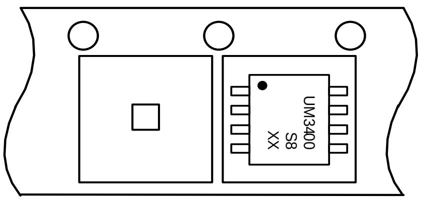

| Symbol | DIMENSIONS | | | | | |
|---|---|---|---|---|---|---|
| | MILLIMETERS | | | INCHES | | |
| | Min | Typ | Max | Min | Typ | Max |
| A | 1.35 | 1.55 | 1.75 | 0.053 | 0.061 | 0.069 |
| A1 | 0.10 | - | 0.25 | 0.004 | - | 0.010 |
| A2 | 1.25 | - | 1.65 | 0.049 | - | 0.065 |
| b | 0.30 | - | 0.51 | 0.012 | - | 0.020 |
| c | 0.15 | - | 0.25 | 0.006 | - | 0.010 |
| D | 4.70 | 4.90 | 5.10 | 0.185 | 0.193 | 0.200 |
| E | 3.80 | 3.90 | 4.00 | 0.150 | 0.154 | 0.157 |
| E1 | 5.80 | 6.00 | 6.20 | 0.228 | 0.236 | 0.244 |
| e | 1.27BSC | | | 0.050 BSC | | |
| L | 0.40 | - | 1.27 | 0.016 | - | 0.050 |
| θ | 0° | - | 8° | 0° | - | 8° |

**Land Pattern**



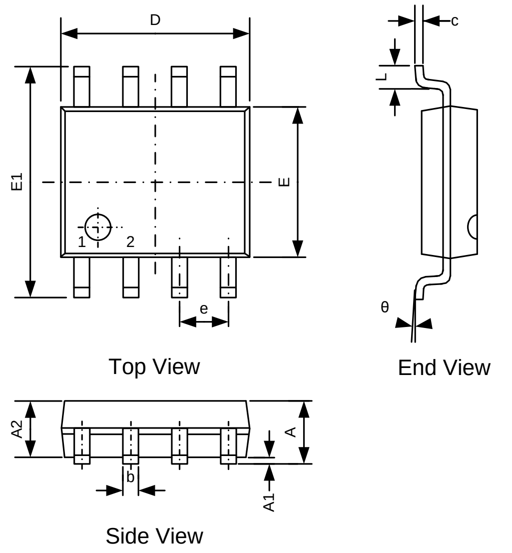

NOTES:
1. Compound dimension: 4.90×3.90.
2. Unit: mm.
3. General tolerance ±0.05mm unless otherwise specified.
4. The layout is just for reference.

**Tape and Reel Orientation**



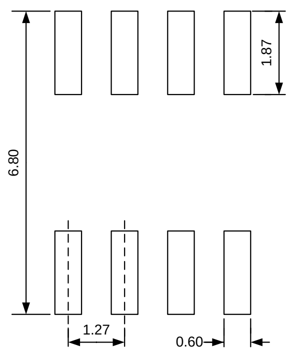
## UM3401 SOP8

### Outline Drawing



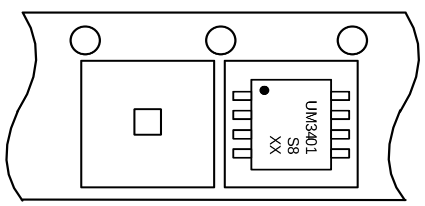

| Symbol | DIMENSIONS MILLIMETERS Min | Typ | Max | INCHES Min | Typ | Max |
|---|---|---|---|---|---|---|
| A | 1.35 | 1.55 | 1.75 | 0.053 | 0.061 | 0.069 |
| A1 | 0.10 | - | 0.25 | 0.004 | - | 0.010 |
| A2 | 1.25 | - | 1.65 | 0.049 | - | 0.065 |
| b | 0.30 | - | 0.51 | 0.012 | - | 0.020 |
| c | 0.15 | - | 0.25 | 0.006 | - | 0.010 |
| D | 4.70 | 4.90 | 5.10 | 0.185 | 0.193 | 0.200 |
| E | 3.80 | 3.90 | 4.00 | 0.150 | 0.154 | 0.157 |
| E1 | 5.80 | 6.00 | 6.20 | 0.228 | 0.236 | 0.244 |
| e | 1.27BSC | | | 0.050 BSC | | |
| L | 0.40 | - | 1.27 | 0.016 | - | 0.050 |
| θ | 0 ° | - | 8 ° | 0 ° | - | 8 ° |

### Land Pattern

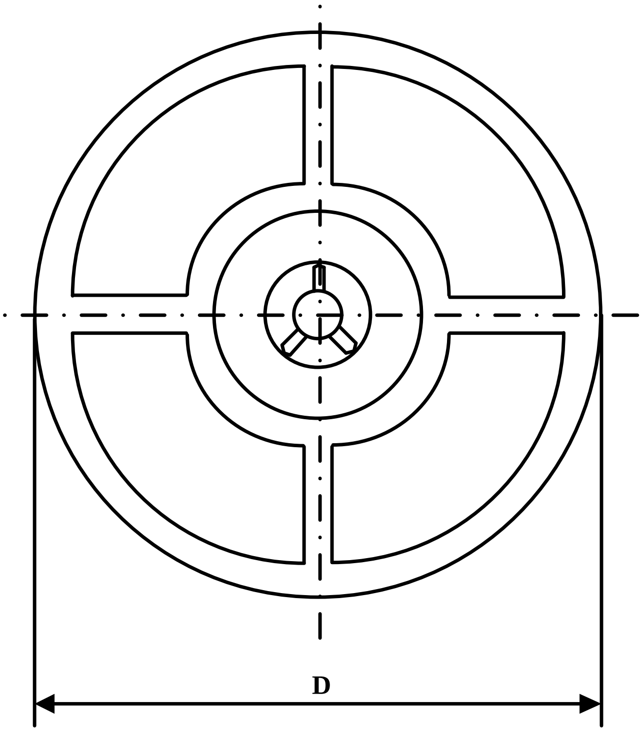


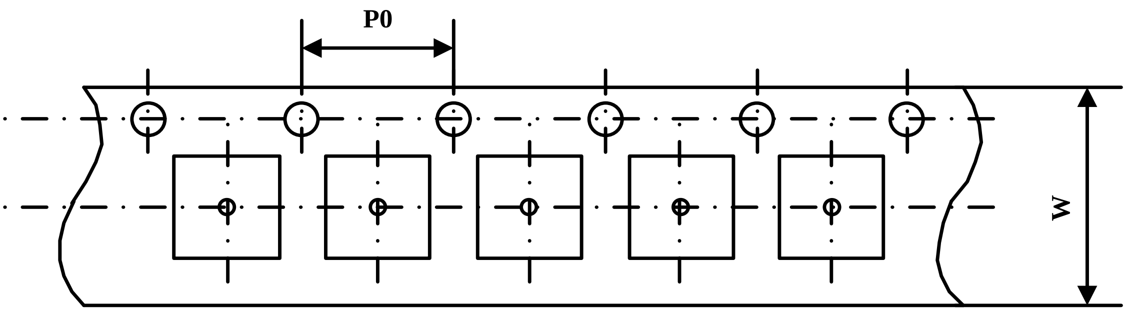

NOTES:
1. Compound dimension: 4.90×3.90.
2. Unit: mm.
3. General tolerance ±0.05mm unless otherwise specified.
4. The layout is just for reference.

### Tape and Reel Orientation



## Packing Information




| Part Number | Package Type | Carrier Width(W) | Pitch(P0) | Reel Size(D) |
|---|---|---|---|---|
| UM400S8 | SOP8 | 12 mm | 4 mm | 330 mm |
| UM3401S8 | SOP8 | 12 mm | 4 mm | 330 mm |

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