

低压、双通道单刀双掷 (SPDT) 模拟开关

UM3257 DFN12 3.0×1.6

描述

UM3257 是一款双通道、单刀双掷 (SPDT) 模拟开关，采用硅栅 CMOS 技术制造。该器件在保持 CMOS 低功耗的同时，具备极低的传播延迟和导通电阻。这使其成为便携式和电池供电应用的理想选择。

UM3257 在开关打开时可在电源轨内以优异的性能双向传输信号，而在关闭时则可阻断高达电源电平的信号，同时保证先断后连的功能。

该器件的选择引脚具有过压保护功能，无论工作电压是多少，都允许该引脚上的电压高于 V_{CC} ，最高可达 6.5V，而不会造成损坏或中断部件的运行。

UM3257 通过改变控制电路的输入缓冲器，只要将控制信号的输入保持在大于 V_{IH} 的最小值和小于 V_{IL} 的最大值，就能保持轨对轨信号传输时的低功耗。因此，该器件可在混合电压轨环境中使用，特别是在手机应用中，可与基带处理器的通用 I/O 直接连接，不再需要将控制引脚输入等同于 V_{CC} ，以保持低功耗。

UM3257 采用符合 ROHS 标准的 12 引脚 DFN12 封装。尺寸为 3.0×1.6mm。引脚间距为 0.5 mm，表面镀有无铅镍钎。小型化封装使其非常适合用于手机、数码相机和 PDA 等便携式电子产品。

应用

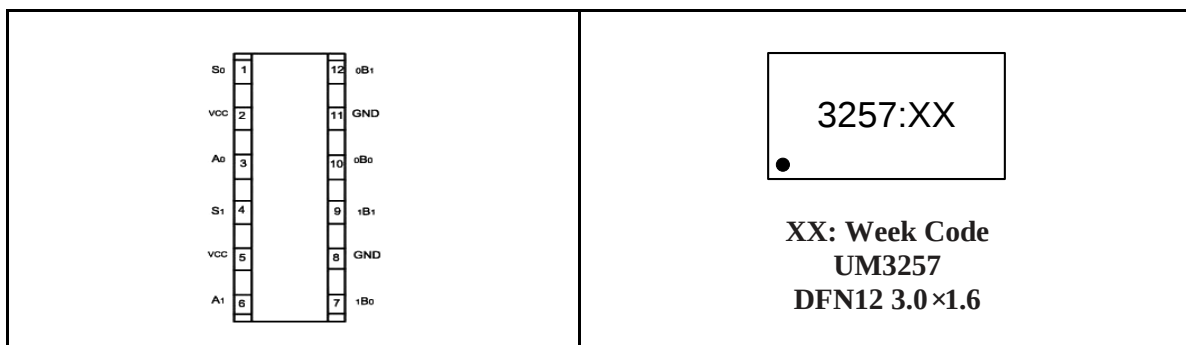
- 采样和保持电路
- 电池供电设备
- 音频和视频信号路由
- 通信电路

特性

- S 管脚输入电平在要求的 V_{IH} 和 V_{IL} 范围内时 I_{CC} 较低
- 低导通电阻 (10Ω)
- 控制引脚输入为 5V 耐压
- 低电荷注入
- 极佳的通道间导通电阻匹配
- 低总谐波失真
- 1.65V 至 5.5V 单电源运行
- ESD 性能：
人体放电模型 (HBM) >2kV
机器放电模型 (MM) >200V
- 采用 DFN12 封装
- 无铅封装

引脚配置

顶部视图



Ordering Information

Part Number	Packaging Type	Marking Code	Shipping Qty
UM3257	DFN12 3.0×1.6	3257	3000pcs/7 Inch Tape & Reel

Function Table

Select Input	Function
L	B0 Connected to A
H	B1 Connected to A

Absolute Maximum Ratings

Symbol	Parameter	Limit	Unit
V_{CC}	Supply Voltage	-0.5 to +6.5	V
V_{IS}	DC Switch Input Voltage (Note 1)	-0.5 to ($V_{CC}+0.5$)	
V_{IN}	DC IN Voltage (Note 1)	-0.5 to +6.5	
I_{IK}	DC Input Diode Current @ $V_{IN}<0V$	-50	mA
I_{OUT}	DC Output Current	128	
I_{CC}/I_{GND}	DC V_{CC} or Ground Current	+100	
T_J	Junction Temperature Under Bias	+150	°C
T_{STG}	Storage Temperature	-65 to +150	
T_L	Junction Lead Temperature (Soldering, 10 Seconds)	260	
θ_{JA}	Thermal Resistance	350	°C/W
P_D	Power Dissipation @ +85 °C	180	mW

Note 1: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Recommended Ratings (Note2)

Symbol	Parameter	Limit	Unit
V_{CC}	Supply Voltage Operating	1.65 to 5.5	V
V_{IS}	Switch Input Voltage	0 to V_{CC}	
V_{IN}	Select Input Voltage	0 to V_{CC}	
V_{OUT}	Output Voltage	0 to V_{CC}	
T_A	Operating Temperature	-55 to +125	°C
t_r, t_f	Input Rise and Fall Time Control Input $V_{CC}=2.3V$ to 3.6V Control Input $V_{CC}=4.5V$ to 5.5V	0 to 10 0 to 5.0	ns/V

Note 2: Select input must be held HIGH or LOW, it must not float.

Electrical Characteristics

Symbol	Parameter	Test Conditions	V _{CC} (V)	Temp	Limits (–40 °C to 85 °C)			Unit
					Min	Typ	Max	
DC Electrical Characteristics								
	Analog Signal Range		V _{CC}	Full	0		V _{CC}	V
I _{IN}	Input Leakage Current	0≤V _{IN} ≤5.5V	0 to 5.5	Room Full		±0.05	±0.1 ±1	μA
I _{OFF}	OFF State Leakage Current	0≤A, B≤V _{CC}	1.65 to 5.5	Room Full		±0.05	±0.1 ±1	μA
V _{IH}	Input High Voltage		1.65 to 1.95 2.3 to 5.5	Full	0.75V _{CC} 0.7V _{CC}			V
V _{IL}	Input Low Voltage		1.65 to 1.95 2.3 to 5.5	Full			0.25V _{CC} 0.3V _{CC}	V
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _O =0	5.5	Room Full			1.0 10	μA
R _{ON}	On-Resistance (Note3)	V _{IN} =0V, I _O =30mA V _{IN} =2.4V, I _O =-30mA V _{IN} =4.5V, I _O =-30mA	4.5	Full		3.0 5.0 7.0	6.0 8.0 13	Ω
		V _{IN} =0V, I _O =24mA V _{IN} =3V, I _O =-24mA	3.0	Full		4.0 10	8.0 19	
		V _{IN} =0V, I _O =8mA V _{IN} =2.3V, I _O =-8mA	2.3	Full		5.0 13	9.0 24	
		V _{IN} =0V, I _O =4mA V _{IN} =1.65V, I _O =-4mA	1.65	Full		6.5 17	12 39	
R _{RANGE}	On Resistance Over Signal Range (Note3, 7)	I _A =-30mA , 0≤V _{Bn} ≤V _{CC}	4.5	Full			25	Ω
		I _A =-24mA, 0≤V _{Bn} ≤V _{CC}	3.0	Full			50	
		I _A =-8mA, 0≤V _{Bn} ≤V _{CC}	2.3	Full			100	
		I _A =-4mA, 0≤V _{Bn} ≤V _{CC}	1.65	Full			300	
ΔR _{ON}	On Resistance Match Between Channels (Note3, 4, 5)	I _A =-30mA, V _{Bn} = 3.15V	4.5	Room		0.15		Ω
		I _A =-24mA, V _{Bn} = 2.1V	3.0	Room		0.2		
		I _A =-8mA, V _{Bn} = 1.6V	2.3	Room		0.5		
		I _A =-4mA, V _{Bn} = 1.15V	1.65	Room		0.5		
R _{FLAT}	On Resistance Flatness (Note3, 4, 6)	I _A =-30mA, 0≤V _{Bn} ≤V _{CC}	5.0	Room		5.0		Ω
		I _A =-24mA, 0≤V _{Bn} ≤V _{CC}	3.3	Room		10		
		I _A =-8mA, 0≤V _{Bn} ≤V _{CC}	2.5	Room		24		
		I _A =-4mA, 0≤V _{Bn} ≤V _{CC}	1.8	Room		110		

Note 3: Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B Ports).

Note 4: Parameter is characterized but not tested in production.

Note 5: ΔR_{ON} = | R_{ON (A00Bn)} – R_{ON (A11Bn)} | measured at identical V_{CC}, temperature and voltage levels.

Note 6: Flatness is defined as the difference between the maximum and minimum value of On Resistance over the specified range of conditions.

Note 7: Guaranteed by design.

Electrical Characteristics (Continued)

Symbol	Parameter	Test Conditions	V _{CC} (V)	Temp	Limits (–40 °C to 85 °C)			Unit
					Min	Typ	Max	
AC Electrical Characteristics								
t _{PHL} t _{PLH}	Propagation Delay Bus to Bus (Note 9)	V _I =OPEN	1.65 to1.95 2.3 to 2.7 3.0 to 3.6 4.5 to 5.5	Room		1.2 0.8 0.3		ns
t _{PZL} t _{PZH}	Output Enable Time Turn On Time (A to Bn)	V _I =2×V _{CC} for t _{PZL} V _I =0V for t _{PZH}	1.65 to1.95 2.3 to 2.7 3.0 to 3.6 4.5 to 5.5	Full	7.0 3.5 2.5 1.7		32 14 7.6 5.7	ns
t _{PLZ} t _{PHZ}	Output Disable Time Turn Off Time (A Port to B Port)	V _I =2×V _{CC} for t _{PLZ} V _I =0V for t _{PHZ}	1.65 to1.95 2.3 to 2.7 3.0 to 3.6 4.5 to 5.5	Full	3.0 2.0 1.5 0.8		28 15 11 8	ns
t _{BBM}	Break Before Make Time (Note 8)	R _L =50Ω, C _L =35pF	1.65 to1.95 2.3 to 2.7 3.0 to 3.6 4.5 to 5.5	Full	0.5 0.5 0.5 0.5			ns
Q _{INJ}	Charge Injection (Note 8)	C _L =0.1nF, V _{GEN} =0V, R _{GEN} =0Ω	5.0 3.3	Room		7.0 3.0		pC
O _{IRR}	Off Isolation (Note 10)	R _L =50Ω, f=10 MHz	1.65 to 5.5	Room		-55		dB
Xtalk	Crosstalk	R _L =50Ω, f=10 MHz	1.65 to 5.5	Room		-54		dB
BW	-3dB Bandwidth	R _L =50Ω	2.5 to 5.5	Room		250		MHz
THD	Total Harmonic Distortion (Note8)	R _L =600Ω, 0.5V _{P-P} , f=600Hz to 20kHz	2.5 5.0	Room		0.014 0.004		%
Capacitance								
C _{IN}	IN Pin Input Capacitance (Note11)	V _{CC} =0V				2.3		pF
C _{IO-B}	B Port Off Capacitance (Note11)	V _{CC} =5.0V				6.5		pF
C _{IOA-ON}	A Port Capacitance when Switch is Enabled (Note11)	V _{CC} =5.0V				18.5		pF

Note 8: Guaranteed by design.

Note 9: This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On Resistance of the switch and the 35 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

Note 10: Off Isolation=20log₁₀ [V_A/V_{Bn}].

Note 11: T_A=+25 °C, f=1MHz, Capacitance is characterized but not tested in production.

Test Circuits/Timing Diagrams

NOTE: Input driven by 50 Ω source terminated in 50 Ω
 NOTE: C_L includes load and stray capacitance
 NOTE: Input PRR = 1.0 MHz; $t_W = 500$ ns

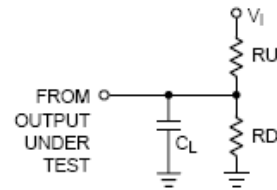


Figure 1 . AC Test Circuit

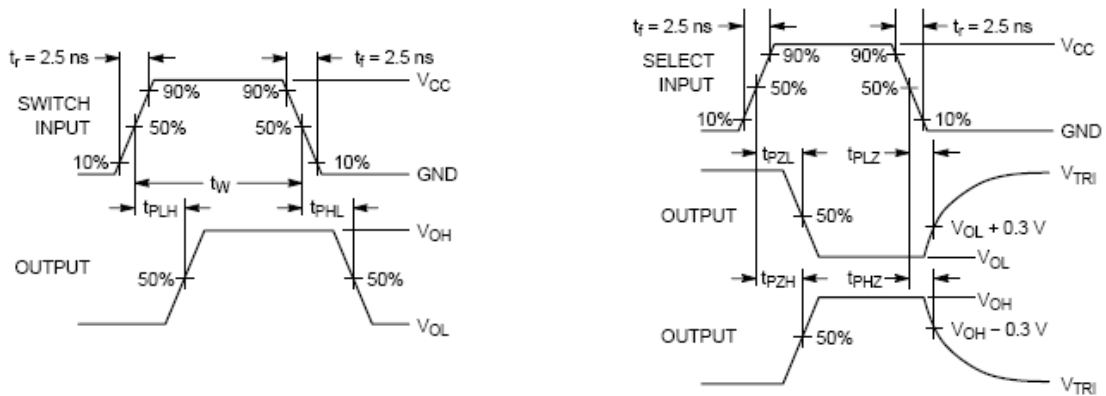
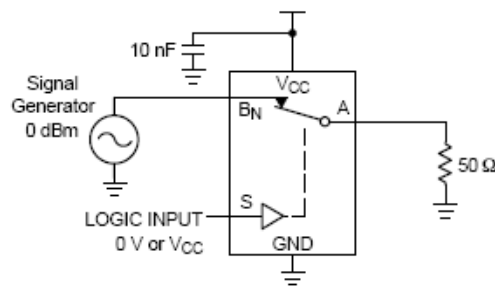
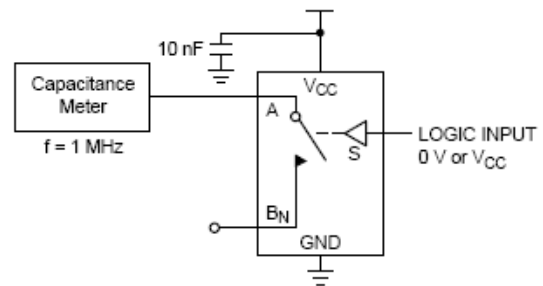
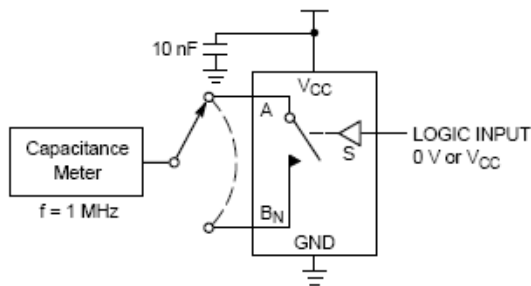
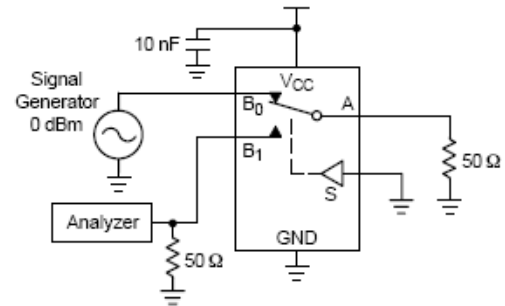
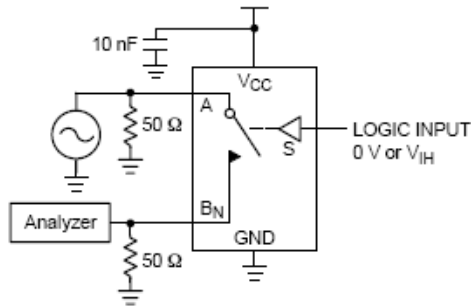
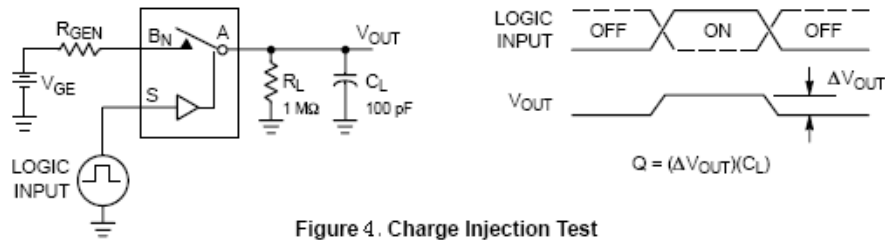


Figure 2 . AC Waveforms

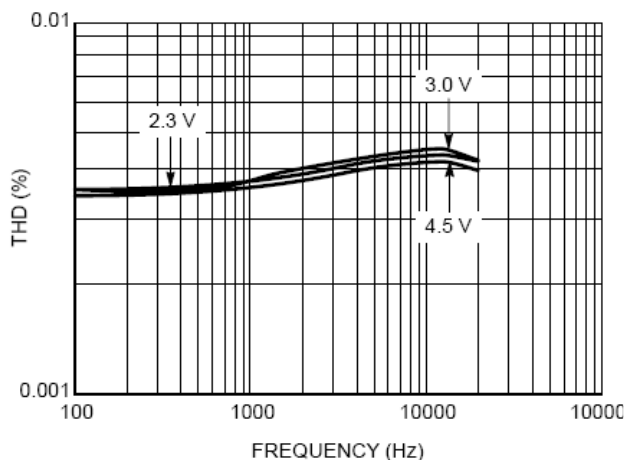


Figure 3 . Break Before Make Interval Timing

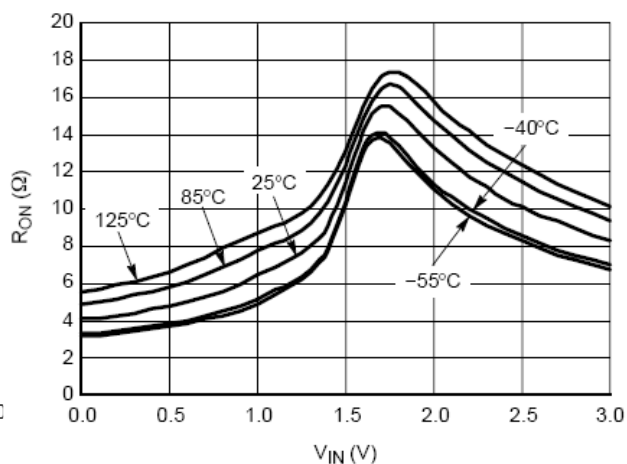


Typical Operating Characteristics

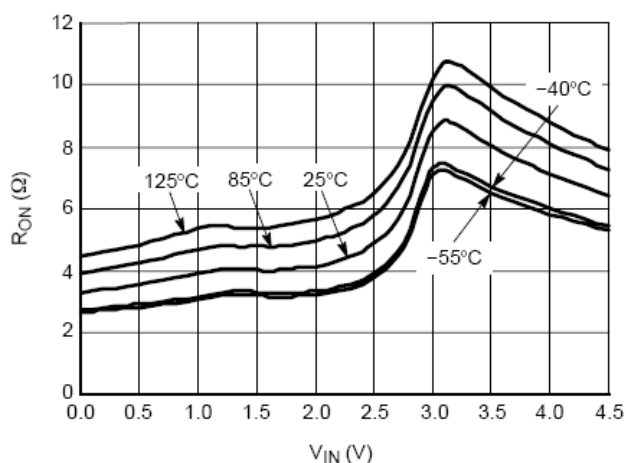
Total Harmonic Distortion vs. Frequency



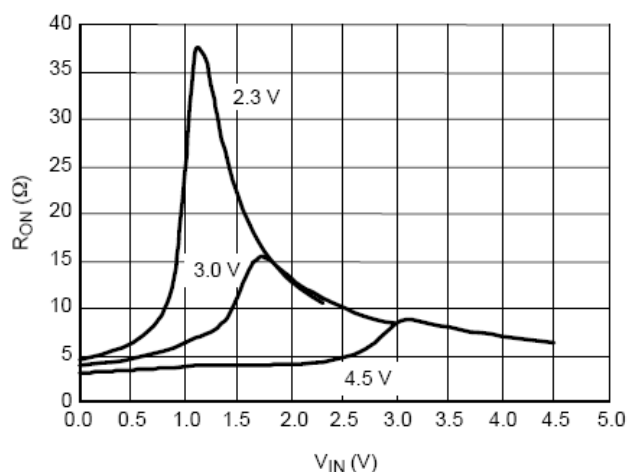
R_{ON} vs. V_{IN} vs. Temperature @ $V_{CC}=3.0V$



R_{ON} vs. V_{IN} vs. Temperature @ $V_{CC}=4.5V$

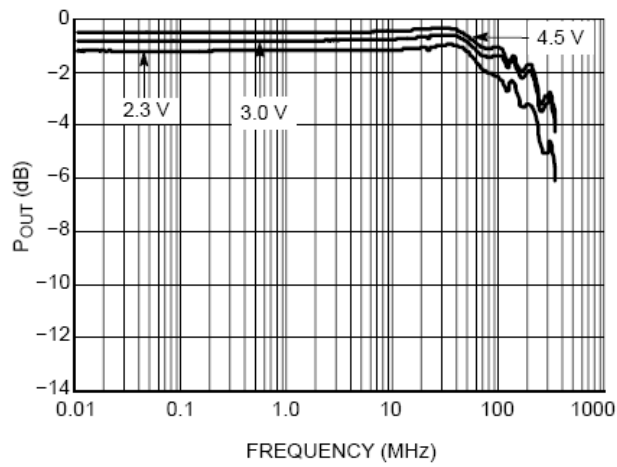


On-Resistance vs. Input Voltage

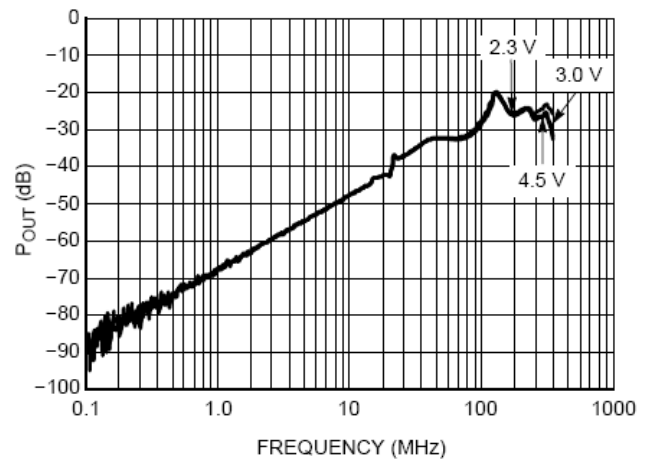


Typical Operating Characteristics (Continued)

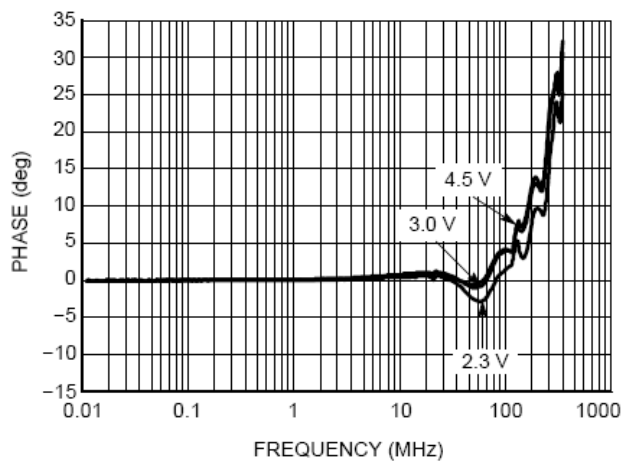
Bandwidth vs. Frequency



Off-Isolation vs. Frequency



Phase Angle vs. Frequency



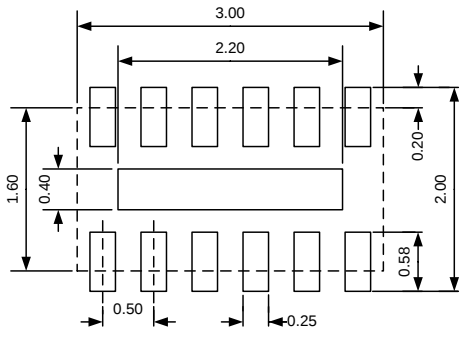
Package Information

UM3257 DFN12 3.0×1.6

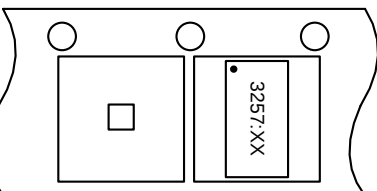
Outline Drawing

DIMENSIONS						
Symbol	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	0.50	0.55	0.605	0.020	0.022	0.024
A1	0.00	-	0.05	0.000	-	0.002
A3	0.15REF			0.006REF		
b	0.20	0.25	0.30	0.008	0.010	0.012
D	2.95	3.00	3.075	0.116	0.118	0.121
D2	2.10	2.20	2.30	0.083	0.087	0.091
E	1.55	1.60	1.675	0.061	0.063	0.066
E2	0.25	-	0.50	0.010	-	0.020
e	0.50TYP			0.020TYP		
L	0.23	-	0.38	0.009	-	0.015

Land Pattern

	NOTES: - Compound dimension: 3.00×1.60; - Unit: mm; - General tolerance $\pm 0.05\text{mm}$ unless otherwise specified; - The layout is just for reference.
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Tape and Reel Orientation

	
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