

±15kV ESD 保护、失效保护、热插拔 自动极性反转RS-485 收发器

UM3089E *SOP14*

描述

UM3089E系列是具有+5.0V供电、±15kV ESD保护、失效保护、热插拔、自动极性反转的 RS-485收发器。这些器件具有失效保护电路,可在接收器输入开路、短路或闲置时确保接 收器输出为逻辑高电平。这意味着如果端接总线上的所有发射器都被禁用(高阻抗),接 收器输出将为逻辑高电平。UM3089E具有低摆率驱动器,可充分降低EMI并减少因电缆端接不当引起的反射,从而实现高达500kbps的无误差数据传输。所有发射器输出和接收器输入能够耐受±8kV的人体模型放电和±15kV的IEC61000-4-2 空气间隙放电。

UM3089E具备电缆自动反转功能,可在电缆连接错误时反转RS-485总线引脚的极性。即使接收器极性反转,也能保持接收器的完整故障安全功能。

这些收发器在空载时或满载禁用驱动器时的典型电源电流消耗为300μA。所有器件都具有 1/8单位负载接收器输入阻抗,支持总线连接多达256个收发器,适用于半双工通信。该器件 还具有过流保护和热关断保护。

应用

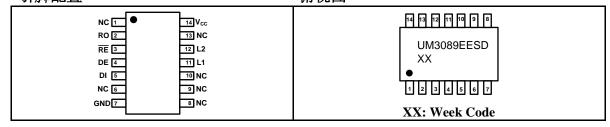
- 空调、建筑照明和环境控制系统
- 工业控制局域网
- PROFIBUS 和其他基于 RS-485 的 现场总线网络
- 多节点数 RS-485 系统
- 适用于 EMI 敏感应用的收发器
- 智能电表/自动抄表系统

特性

- 自动极性反转 RS-485 收发器
- 1μA 关机电流和 300μA 接收器电流
- 真正的故障安全接收器和热插拔功能
- 增强型压摆率限制
- 支持总线连接多达 256 个收发器
- 热关断
- 驱动过载限流保护
- RS-485 I/O 引脚提供 ESD 保护
 - ±15kV—IEC61000-4-2 空气间隙放电
 - ±8kV—IEC61000-4-2 接触放电

引脚配置

俯视图



订购信息

Part Number	Marking Code	Package Type	Shipping Qty	
UM3089EESD	UM3089EESD	SOP14	2500pcs/13 Inch Tape & Reel	



Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	+7	V
	Control Input Voltage (RE, DE)	$-0.3V$ to $(V_{CC} + 0.3V)$	V
	Driver Input Voltage (DI)	$-0.3V$ to $(V_{CC} + 0.3V)$	V
	Driver Output Voltage (L1, L2)	-7.5 to +12.5	V
	Receiver Input Voltage (L1, L2)	-7.5 to +12.5	V
	Receiver Output Voltage (RO)	$-0.3V$ to $(V_{CC} + 0.3V)$	V
T_A	Ambient Temperature	-40 to +85	${\mathcal C}$
T_{STG}	Storage Temperature Range	-65 to +160	${\mathcal C}$
$T_{\rm L}$	Lead Temperature for Soldering 10 seconds	+300	${\mathcal C}$

DC Electrical Characteristics

(V_{CC} = +5V \pm 5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V and T_A = +25 °C.) (Note 1)

Parameter	Symbol	Test Conditions		Min	Тур	Max	Unit
SUPPLY CURRENT							
Supply Current	$ m I_{CC}$	No load, DI = GND	$DE = V_{CC},$ $\overline{RE} = 0V \text{ or } V_{CC}$	0.3			mA
a approximation		or V _{CC}	$DE = 0V,$ $\overline{RE} = 0V$	0.25			
Supply Current in Shutdown Mode	I_{SHDN}	DE = G	ND, $\overline{RE} = V_{CC}$	0.002		10	μА
LOGIC							
Input High Voltage	V_{IH1}	DE.	, DI, RE	2.0			V
Input Low Voltage	V_{IL1}	DE, DI, RE				0.4	V
DI Input Hysteresis	V_{HYS}				300		mV
DRIVER							
Differential Driver Output	V_{OD1}	No Lo	oad, Figure 2	4.9		5	V
Differential Driver Output	V_{OD2}	Figure	$2, R_L = 54\Omega$	2.0	2.2		V
Change-in-Magnitude of Differential Output Voltage	ΔV_{OD}	Figure 2, R_L = 54 Ω ; (Note 2)				0.1	V
Driver Common-Mode Output Voltage	V _{oc}	Figure 2, $R_L = 54\Omega$			2.2	2.5	V
Change-in-Magnitude of Common-Mode Voltage	ΔV_{OC}	_	2 , $R_L = 54\Omega$; Note 2)			0.1	V
Driver Short-Circuit Output	т	Vo	$_{\mathrm{UT}} = -7\mathrm{V}$		-250		mA
Current (Note 3)	I_{OSD}	Vol	$_{\rm UT} = 12V$		250		IIIA

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DC Electrical Characteristics (Continued)

(V_{CC} = +5V ±5%, T_A = T_{MIN} to T_{MAX} , unless otherwise noted. Typical values are at V_{CC} = +5V and T_A = +25 °C.) (Note 1)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
RECEIVER							
Receiver Differential Threshold Voltage	V_{TH}	-7V≤V _{CM} ≤12V		-200		-50	mV
Receiver Input Hysteresis	ΔV_{TH}	V _{CM} =0V			25		mV
Receiver Input Resistance	R_{IN}	-7V≤V	_{CM} ≤12V	96			kΩ
Input Current (L1 and L2)	ī	DE = GND,	$V_{IN} = 12V$		0.1	1.0	mA
input Current (E1 and E2)	I_{IN2}	$V_{CC} = GND$ or $5V$	$V_{\rm IN} = -7V$		0.08	-0.8	IIIA
Receiver Output High Voltage	V_{OH}	$I_{O} = -1.5 \text{mA}, V_{ID} = 200 \text{mV}$		V _{CC} -1.5			V
Receiver Output Low Voltage	V _{OL}	$I_{O} = 2.5 \text{mA}, V_{ID} = -200 \text{mV}$				0.4	V
Three-State Output Current at Receiver	I_{OZR}	$0V \le V_O \le V_{CC}$				±1	μΑ
Receiver Output Short Circuit Current	I_{OSR}	$0V \le V_{RO} \le V_{CC}$		±8		±60	mA
Thermal Shutdown Temperature	$\mathrm{T}_{\mathrm{SHDN}}$				140		С
Thermal Shutdown Hysteresis	$\triangle T_{SHDN}$				20		\mathcal{C}
ESD Protection				<u>. </u>			
		Human B	ody Model		<u>±</u> 8		
ESD Protection for L1, L2		IEC61000-4-2 Air-Gap Discharge			±15		kV
			-4-2 Contact charge		<u>±</u> 8		

Note 1: All currents into the device are positive; all currents out of the device are negative. All voltages are referred to device ground unless otherwise noted.

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Note 2: ΔV_{OD} and ΔV_{OC} are the changes in V_{OD} and V_{OC} , respectively, when the DI input changes state.

Note 3: Maximum current level applies to peak current just prior to fold back current limiting; minimum current level applies during current limiting.



Switching Characteristics

(V_{CC} = +5V \pm 5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V and T_A = +25 °C.)

Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit
Maximum Data Rate	f_{MAX}			500		kbps
Driver Input-to-Output	t _{DPLH}	Figures 3 and 7, $R_{DIFF} = 54\Omega$,	50	100	200	ns
Driver input-to-Output	t_{DPHL}	$C_{L1} = C_{L2} = 100 pF$	50	100	200	118
Driver Output Skew t _{DPLH} - t _{DPHL}	t _{DSKEW}	Figures 3 and 7, $R_{DIFF} = 54\Omega$, $C_{L1} = C_{L2} = 100 pF$		3	100	ns
Driver Rise or Fall Time	$t_{\mathrm{DR}},t_{\mathrm{DF}}$	Figures 3 and 7, $R_{DIFF} = 54\Omega$, $C_{L1} = C_{L2} = 100 pF$	100	200	500	ns
Driver Enable to Output High	t _{DZH}	Figures 4 and 8, $C_L = 100 pF$, S2 closed		100	2500	ns
Driver Enable to Output Low	t _{DZL}	Figures 4 and 8, $C_L = 100 pF$, S1 closed		100	2500	ns
Driver Disable Time from Low	t _{DLZ}	Figures 4 and 8, $C_L = 15 pF$, S1 closed		50	100	ns
Driver Disable Time from High	$t_{ m DHZ}$	Figures 4 and 8, $C_L = 15 pF$, S2 closed		50	100	ns
Receiver Input to Output	t _{RPLH} , t _{RPHL}	$\begin{array}{c} \mid V_{ID} \mid \geq 2.0V; \\ \text{rise and fall time of } V_{ID} \leq 15 \text{ns} \end{array}$		100	200	ns
Differential Receiver Skew t _{RPLH} - t _{RPHL}	t _{RSKD}	Figures 6 and 9; $ V_{ID} \ge 2.0V$; rise and fall time of $V_{ID} \le 15$ ns		4	30	ns
Receiver Enable to Output Low	t _{RZL}	Figures 5 and 10, $C_L = 100 pF$, S1 closed		20	200	ns
Receiver Enable to Output High	t _{RZH}	Figures 5 and 10, $C_L = 100 pF$, S2 closed		20	200	ns
Receiver Disable Time from Low	t _{RLZ}	Figures 5 and 10, $C_L = 100 pF$, S1 closed		20	200	ns
Receiver Disable Time from High	$t_{ m RHZ}$	Figures 5 and 10, $C_L = 100 pF$, S2 closed		20	200	ns
Time to Shutdown	t_{SHDN}	(Note 4)	50	200	600	ns
Driver Enable from Shutdown to Output High	t _{DZH(SHDN)}	Figures 4 and 8, $C_L = 15 pF$, S2 closed			4500	ns
Driver Enable from Shutdown to Output Low	$t_{\rm DZL(SHDN)}$	Figures 4 and 8, $C_L = 15 pF$, S1 closed			4500	ns
Receiver Enable from Shutdown to Output High	$t_{RZH(SHDN)}$	Figures 5 and 10, $C_L = 100 pF$, S2 closed			3500	ns
Receiver Enable from Shutdown to Output Low	$t_{RZL(SHDN)}$	Figures 5 and 10, $C_L = 100 pF$, S1 closed			3500	ns

Note 4: The device is put into shutdown by bringing \overline{RE} high and DE low. If the enable inputs are in this state for less than 50ns, the device is guaranteed not to enter shutdown. If the enable inputs are in this state for at least 600ns, the device is guaranteed to have entered shutdown.



Non-Polarity Features

The Polarities of driver and receiver are always kept the same status. When $DE=\overline{RE}=LOGIC\ 0$ and RO is standing LOGIC 0 for T_S time, the polarities will be reversed automatically.

Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit
Waiting Time for Inverting	$T_{\rm s}$	$DE=\overline{RE}=L$, RO keeps L	150	200	250	ms

Pin Description

Pin Number	Symbol	Function
1	NC	Not Connected.
2	RO	Receiver Output.
3	\overline{RE}	Receiver Enable. Drive \overline{RE} low to enable receivers, RO is high impedance when \overline{RE} is high. Drive \overline{RE} high and DE low to enter low-power shutdown mode.
4	DE	Driver Enable. Drive DE high to enable drivers. The outputs are high impedance when DE is low. Drive \overline{RE} high and DE low to enter low-power shutdown mode.
5	DI	Driver Input
6	NC	Not Connected.
7	GND	Ground
8	NC	Not Connected.
9	NC	Not Connected.
10	NC	Not Connected.
11	L1	RS485 Receiver Input and Driver Output Pin. Normally L2 is non-inverting bus I/O for transceiver (referred as A in traditional RS485 transceiver) and L1 is inverting bus I/O for transceiver
12	L2	(referred as B in traditional RS485 transceiver). Under polarity reversal status, L2 becomes inverting bus I/O and L1 becomes non-inverting bus I/O.
13	NC	Not Connected.
14	V_{CC}	Power Supply for RS-485 Transceiver



RS-485 Communication Function Table

Table 1. Transmitting

INPUTS			OUTPUTS		
\overline{RE}	DE	DI	A	В	
X	Н	H/O	Н	L	
X	Н	L	L	Н	
L	L/O	X	Z	Z	
Н	L/O	X	Shutdown		

Table2. Receiving

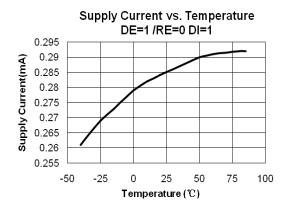
	INPUTS				
RE	DE	$V_{ID}=V_A-V_B$	RO		
L	X	≥-50mV	Н		
L	X	≤-200mV	L		
L	X	Open/Shorted	Н		
Н	Н	X	Z		
Н	L	X	Shutdown		

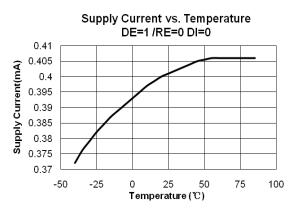
 $\begin{array}{l} \mbox{H: High, L: Low, X: Do not care, Z: High impedance.} \\ \mbox{V_A: Input Voltage of RS485 Non-Inverting Bus I/O terminal,} \\ \mbox{V_B: Input Voltage of RS485 Inverting Bus I/O terminal.} \end{array}$

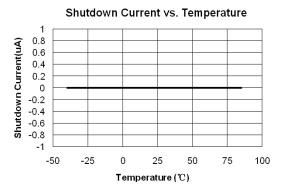


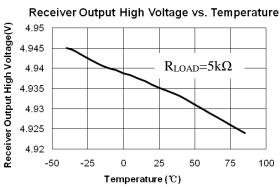
Typical Operating Characteristics

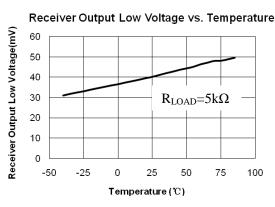
(V_{CC}=5V, driver output and receiver output no load, unless otherwise noted.)

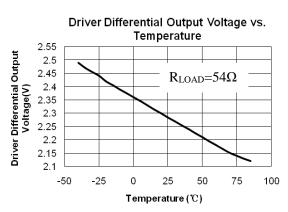


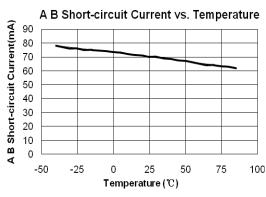


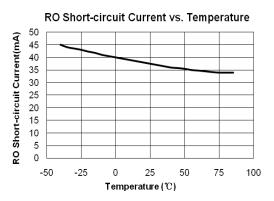








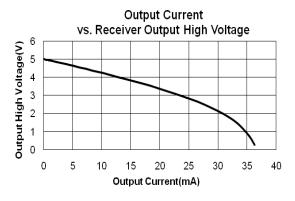


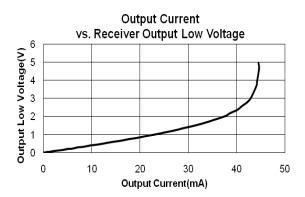


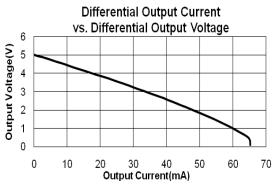


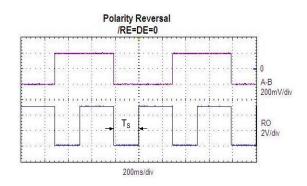
Typical Operating Characteristics (Continued)

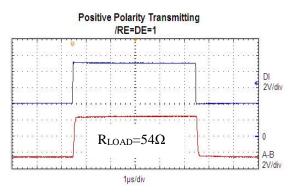
(V_{CC}=5V, driver output and receiver output no load, unless otherwise noted.)

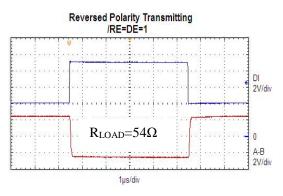


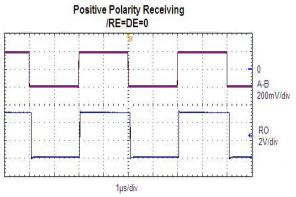


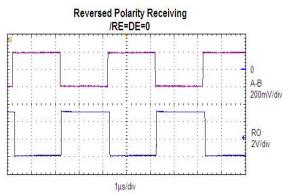














Typical Operating Circuit

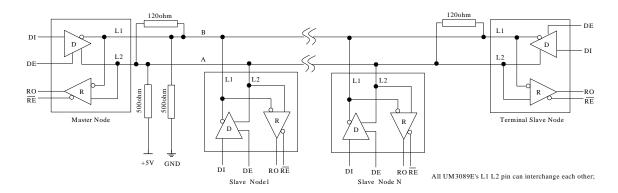


Figure 1. Typical Half-Duplex Non-Polarity RS-485 Network

Test Circuit

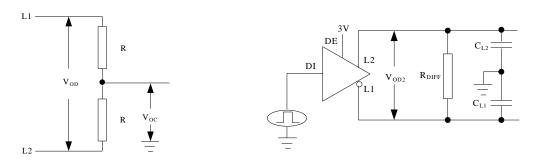


Figure 2. Driver DC Test Load

Figure 3. Driver Timing Test Circuit

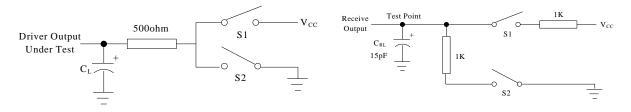


Figure 4. Driver Enable/Disable Timing Test Load Figure 5. Receiver Enable/Disable Timing Test Load



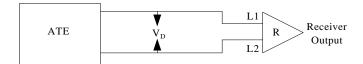


Figure 6. Receiver Propagation Delay Test Circuit

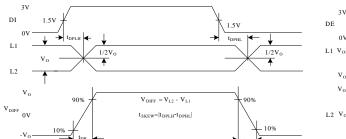


Figure 7. Driver Propagation Delays

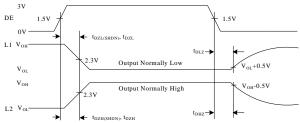


Figure 8. Driver Enable and Disable Times

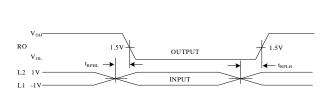


Figure 9. Receiver Propagation Delays

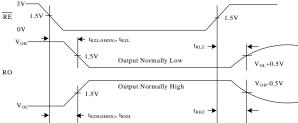


Figure 10. Receiver Enable and Disable Times



Detail Description

Polarity Reversal Function

With large node count RS485 network, it is common for some cable data lines to be wired backwards during installation. When this happens, the node is unable to communicate over network, and must be rewired to the connector, which is time consuming.

The UM3089E simplifies this task by including an automatic polarity reversal function inside.

Upon UM3089E powers up, when $DE=\overline{RE}=logic low$, if RO keeps logic low over a predefined time T_S (i.e $T_S=200ms$ in UM3089E), the chip reverses its bus pins' polarity, so L1 becomes non-inverting, and L2 becomes inverting. Otherwise, the chip operates like any standard RS485 transceiver, and the bus pins have their normal polarity definition of L2 as non-inverting pin and L1 as inverting pin.

Union Semi's unique automatic polarity reversal function is superior to that found on competing devices, because the receiver's full fail safe function is maintained, even when the RX polarity is reversed.

Fail-Safe and Hot-Swap

The UM3089E guarantees a logic high receiver output when the receiver inputs are shorted or open, or when they are connected to a terminated transmission line with all drivers disabled. This is done by setting the receiver input threshold between -50mV and -200mV. If the differential receiver input voltage $V_{\rm ID}$ is greater than or equal to -50mV, RO is logic high. If $V_{\rm ID}$ is less than or equal to -200mV, RO is logic low. In the case of a terminated bus with all transmitters disabled, the receiver's differential input voltage is pulled to 0V by the termination. With the receiver threshold of UM3089E, this results in logic high with a 50mV minimum noise margin, and this -50mV to -200mV threshold complies with the ± 200 mV EIA/TIA-485 standard.

When circuit boards with RS485 transceiver are inserted into a hot or powered backplane, differential disturbances to the data bus can lead to data errors. Upon initial circuit board insertion, the microprocessor undergoes its own power-up sequence. During this period, the processor's

logic output drivers are high impedance and unable to drive the DE and \overline{RE} inputs of these devices to a defined logic level. Leakage currents up to $\pm 10\mu A$ from the high impedance state of processor's logic drivers could cause standard CMOS enable inputs of a transceiver to drift to an incorrect logic level. Additionally, parasitic circuit board capacitance could cause coupling of V_{CC} or GND to the enable inputs. Without the hot-swap capability, these facts could improperly enable the transceiver's driver or receiver.

When V_{CC} rises, an internal pull down circuit holds DE low and \overline{RE} high. After the initial power up sequence, the pull down/pull up circuit becomes transparent, resetting the hot-swap tolerable input. This hot-swap input circuit enhances UM3089E's performance in harsh environment application.

±15kV ESD Protection

All pins on UM3089E device include ESD protection structures, and the family incorporates advanced structures which allow the RS-485 pins (L1, L2) to survive ESD events up to ±15kV. The RS-485 pins are particularly vulnerable to ESD damage because they typically connect to an exposed port on the exterior of the finished product. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. After an ESD event, circuits keep working without latch up. The ESD protection can be tested in various ways and with reference to the ground pin. The L1, L2 are characterized for protection to the following limits: ±8kV using the Human Body Model and ±15kV IEC61000-4-2, Air-Gap Discharge, and ±8kV Contact Discharge.

The logic pins (RO, \overline{RE} , DE, DI) are characterized for protection to the following limits: $\pm 2kV$ using the Human Body Model.



Applications Information

Non-Polarity transceiver

When established the non-polarity RS-485 net, you should pay attention to two conditions. First, a pair of bias resistance (pull-up to +5V for RS-485 A bus, push-down to GND for RS-485 B bus) must be required, usually be built in the master node, or independently, 500Ω resistance is recommended. The other nodes don't need bias resistance anymore. Second, the transceiver rate must be higher than 100bps or the maximum transmitting time for low logic should be less than 100 ms.

256 Transceivers on the Bus

The standard RS-485 receiver input impedance is $12k\Omega$ (one unit load), and the standard driver can drive up to 32 unit loads. The Union family of transceivers have a 1/8 unit load receiver input impedance (96k Ω), allowing up to 256 transceivers to be connected in parallel on one communication line. Any combination of these devices and/or other RS-485 transceivers with a total of 32 unit loads or less can be connected to the line.

Low-Power Shutdown Mode

Low-power shutdown mode is initiated by bringing both \overline{RE} high and DE low. In shutdown, the device typically draws only 10uA of supply current. \overline{RE} and DE may be driven simultaneously; the parts are guaranteed not to enter shutdown if \overline{RE} is high and DE is low for less than 50ns. If the inputs are in this state for at least 600ns, the parts are guaranteed to enter shutdown. Enable times t_{ZH} and t_{ZL} in the Switching Characteristics tables assume the part was not in a low-power shutdown state. Enable times $t_{ZH(SHDN)}$ and $t_{ZL(SHDN)}$ assume the parts were shut down. It takes drivers and receivers longer to become enabled from low-power shutdown mode ($t_{ZH(SHDN)}$), $t_{ZL(SHDN)}$) than from driver/receiver-disable mode (t_{ZH} , t_{ZL}).

Driver Output Protection

Two mechanisms prevent excessive output current and power dissipation caused by faults or by bus contention. The first, a foldback current limit on the output stage, provides immediate protection against short circuits over the whole common-mode voltage range (see Typical Operating Characteristics). The second, a thermal shutdown circuit, forces the driver outputs into a high-impedance state if the die temperature becomes excessive.

Line Length vs. Data Rate

The RS-485/RS-422 standard covers line lengths up to 4000 feet. For line lengths greater than 4000 feet, repeater is required.

Typical Applications

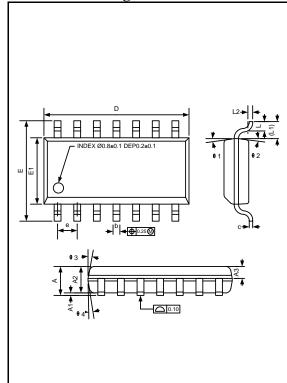
The UM3089E transceivers are designed for bidirectional data communications on multipoint bus transmission lines. To minimize reflections, the line should be terminated at both ends in its characteristic impedance, and stub lengths of the main line should be kept as short as possible.



Package Information

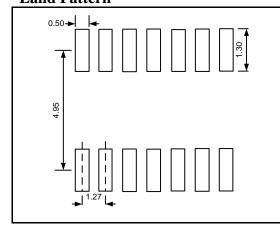
UM3089EESD SOP14

Outline Drawing



DIMENSIONS						
Crombal	MILLIM	1ETERS	INCHES			
Symbol	Min	Max	Min	Max		
A	1.350	1.750	0.053	0.069		
A1	0.100	0.250	0.004	0.010		
A2	1.250	1.650	0.050	0.066		
A3	0.550	0.750	0.022	0.030		
b	0.360	0.510	0.014	0.020		
c	0.170	0.250	0.006	0.010		
D	8.530	8.730	0.341	0.349		
Е	5.800	6.200	0.228	0.244		
E1	3.800	4.000	0.152	0.160		
e	1.270BSC		0.050)BSC		
L	0.450	0.800	0.018	0.032		
L1	1.04	REF	0.042	2REF		
L2	0.250)BSC	0.010)BSC		
θ1	6°	10°	6°	10°		
θ2	6°	10°	6°	10°		
θ3	5°	9°	5°	9°		
θ4	5°	9°	5°	9°		

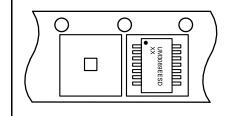
Land Pattern



NOTES:

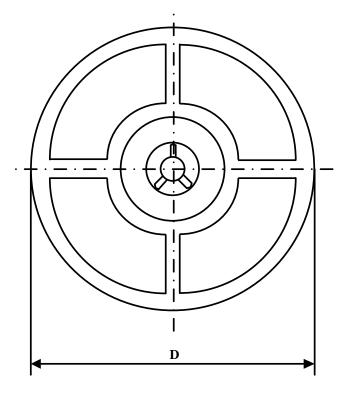
- 1. Compound dimension: 8.63×3.90;
- 2. Unit: mm;
- 3. General tolerance ±0.05mm unless otherwise specified;
- 4. The layout is just for reference.

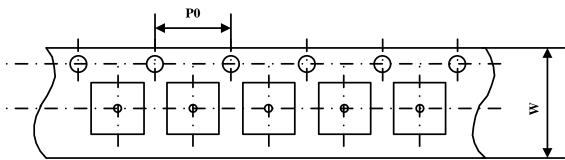
Tape and Reel Orientation





Packing Information





Part Number	Package Type	Carrier Width(W)	Pitch(P0)	Reel Size(D)
UM3089EESD	SOP14	12 mm	4 mm	330 mm



GREEN COMPLIANCE

Union Semiconductor is committed to environmental excellence in all aspects of its operations including meeting or exceeding regulatory requirements with respect to the use of hazardous substances. Numerous successful programs have been implemented to reduce the use of hazardous substances and/or emissions.

All Union components are compliant with the RoHS directive, which helps to support customers in their compliance with environmental directives. For more green compliance information, please visit:

http://www.union-ic.com/index.aspx?cat_code=RoHSDeclaration

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