

用于开漏和推挽应用的2位双向电压电平转换器

UM2102S SOT23-6

描述

UM2102S 允许在 1.5V 和 5V 之间进行双向电压转换而无需使用方向引脚。UM2102S 不是一个总线缓冲器，不能在两侧连接时提供两个电平变换和物理隔离总线任一侧的电平。UM2102S 仅在 VREF 管脚连接到接地时才会隔离两侧。

转换器两侧都需要上拉电阻，以便在转换器总线上提供逻辑高电平。这些上拉电阻的大小取决于系统。除 SMBus 设备外，该器件还可与标准模式、快速模式和快速模式增强型 I²C 总线设备配合使用。最大频率取决于 RC 时间常数，但一般支持 >2MHz。

当 SDA1 或 SDA2 端口为低电平时，通道处于导通状态，SDA1 和 SDA2 端口之间存在低电阻连接。假设 SDA2 端口为更高的电压，当 SDA2 端口为高电平时，SDA1 端口上的电压限制在 V_{CCA} 设置的电压范围内。当 SDA1 端口为高电平时，上拉电阻会将 SDA2 端口拉至漏极上拉电源电压 (V_{CCB})。这一功能允许在用户选择的较高和较低电压之间进行无缝转换，而无需进行方向控制。SCL1/SCL2 通道也可用作 SDA1/SDA2 通道。

所有通道具有相同的电特性，输出间的电压或传输延迟具有最小的偏差。由于开关是对称制造的，所以这有利于分离式晶体管电压变换解决方案。变换器为低电压器件提供极佳的 ESD 保护并同时保护低 ESD 抗性器件。

应用

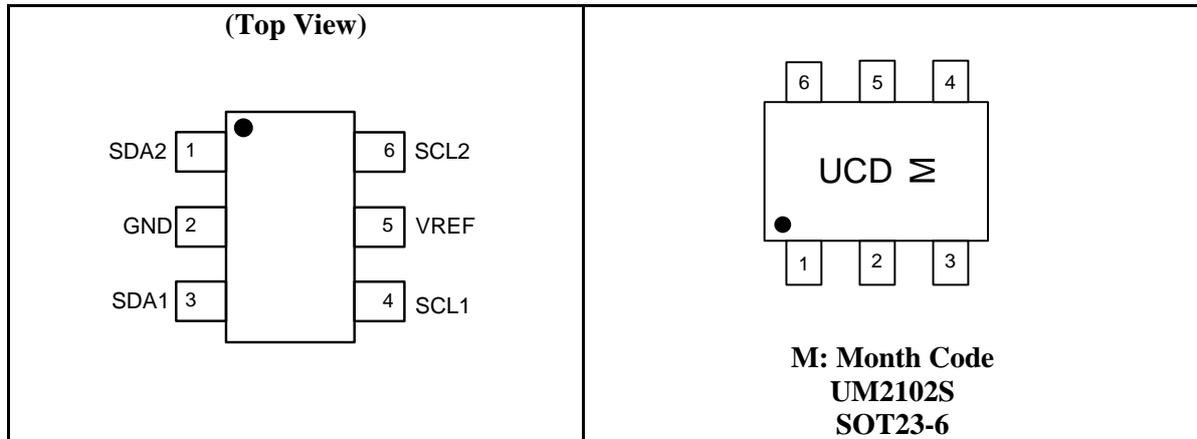
- SPI, SMBus 和 I²C 电平转换
- 低电压 ASIC 电平转换
- 智能读卡器
- 手机支架
- 便携式 POS 系统
- 便携式通信设备
- 低成本串行接口
- 蜂窝电话
- GPS
- 通信设备

特性

- 最大传播延迟小于 3.5ns，可支持标准模式和快速模式 I²C 总线设备及多个主设备
- 开路漏极 I²C 总线 I/O 端口 (SCL1、SDA1、SCL2 和 SDA2)
提供双向电压转换，无方向引脚
- 输入和输出端口之间的低至 3.0Ω 导通状态带来更少的信号失真
- 5V 耐压 I²C 总线 I/O 端口，支持混合模式信号操作
- 无锁定操作
- 直通引出线便于印刷电路板走线排布
- ESD 保护：
 - 根据 JESD22-A114, HBM 超过 2000V
 - 根据 JESD22-A115, MM 超过 200V
 - 根据 JESD22-C101, CDM 超过 1000V
- 可用的封装：SOT23-6

Pin Configurations

Top View



Pin Description

Pin Number	Name	Function
1,6	SDA2,SCL2	High-voltage side; connected to V_{CCB} through a pull-up resistor
2	GND	Ground(0V)
3,4	SDA1,SCL1	Low-voltage side; connected to V_{CCA} through a pull-up resistor
5	V_{REF}	Connected to V_{CCA} to enable the chip and connected to GND to isolate the bus

Ordering Information

Part Number	Packaging Type	Marking Code	Shipping Qty
UM2102S	SOT23-6	UCD	3000pcs/7Inch Tape & Reel

Absolute Maximum Ratings (Note 1)

Over operating free-air temperature range (unless otherwise noted)

Symbol	Parameter		Value	Unit
V_{REF}	Reference Voltage		-0.5 to +6	V
V_I	Input Voltage		-0.5 (Note 2) to +6	V
V_{IO}	Voltage on an Input/Output Pin		-0.5 (Note 2) to +6	V
I_{ch}	Channel Current (DC)		+128	mA
I_{IK}	Input Clamp Current	$V_I < 0V$	-50	mA
T_{stg}	Storage Temperature Range		-65 to +150	°C

Note 1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Note 2: The input and input/output negative voltage ratings may be exceeded if the input and input/output clamp current ratings are observed.

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IO}	Voltage on an Input/Output Pin	SCL1, SDA1, SCL2, SDA2	0	5	V
V_{REF} (Note 3)	Reference Voltage		0	3.6	V
$I_{sw(pass)}$	Pass Switch Current			64	mA
T_{amb}	Ambient Temperature	Operating in Free-Air	-40	+85	°C

Note 3: $V_{REF} (V_{CCA}) \leq V_{CCB} - 1 V$ for best results in level shifting applications.

Electrical Characteristics
 $T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ (Note 4)	Max	Unit	
V_{IK}	Input Clamping Voltage	$I_I = -18\text{mA}$; $V_{REF} = 0\text{V}$			-1.2	V	
I_{IH}	HIGH-Level Input Current	$V_I = 5\text{V}$; $V_{REF} = 0\text{V}$			5	μA	
$C_{io(off)}$	Off-State Input/Output Capacitance	SCLn, SDAn; $V_O = 0\text{V}$ or 3V ; $V_{REF} = 0\text{V}$		10	12.2	pF	
$C_{io(on)}$	On-State Input/Output Capacitance	SCLn, SDAn; $V_O = 0\text{V}$ or 3V ; $V_{REF} = 3\text{V}$		8	12	pF	
R_{on}	ON-State Resistance (Note 5)	SCLn, SDAn; (Note 6) $V_I = 0$; $I_O = 64\text{mA}$	$V_{REF} = 4.5\text{V}$		2.0	5.0	Ω
			$V_{REF} = 3\text{V}$		2.4	6.0	
			$V_{REF} = 2.3\text{V}$		3.1	8.0	
			$V_{REF} = 1.5\text{V}$		11	32	
		SCLn, SDAn; $V_I = 2.4\text{V}$; $I_O = 15\text{mA}$	$V_{REF} = 4.5\text{V}$		4.6	7.5	
			$V_{REF} = 3\text{V}$		50	80	
SCLn, SDAn; $V_I = 1.7\text{V}$; $I_O = 15\text{mA}$	$V_{REF} = 2.3\text{V}$		50	80			

Note 4 : All typical values are at $T_{amb} = 25^{\circ}\text{C}$.

Note 5 : Measured by the voltage drop between the SCL1 and SCL2, or SDA1 and SDA2 terminals at the indicated current through the switch.

ON-state resistance is determined by the lowest voltage of the two terminals.

Note 6 : Guaranteed by design.

Switching Characteristics (Translating Down)

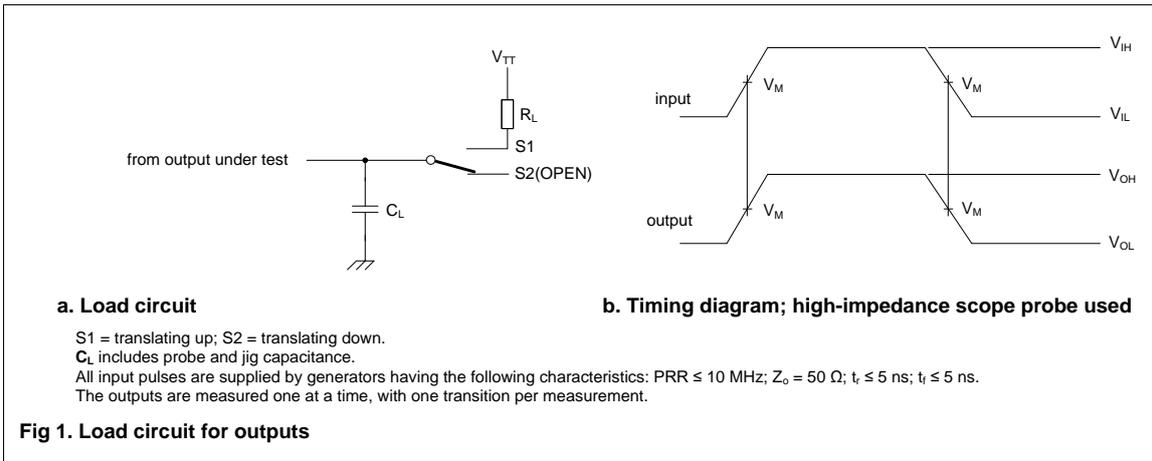
Over recommended operating free-air temperature range (unless otherwise noted). Values guaranteed by design.

Symbol	Parameter	Test Conditions	C _L =50pF		C _L =30pF		C _L =15pF		Unit
			Min	Max	Min	Max	Min	Max	
V _{REF} = 2.3V; V _{IH} = 3.3V; V _{IL} = 0V; V _M = 1.15V (see Figure 1).									
t _{PLH}	LOW to HIGH Propagation Delay	from (Input) SCL2 or SDA2	0	2.5	0	1.7	0	1.2	ns
t _{PHL}	HIGH to LOW Propagation Delay	to (Output) SCL1 or SDA1.	0	2.5	0	2.0	0	1.3	ns
V _{REF} = 1.5V; V _{IH} = 2.5V; V _{IL} = 0V; V _M = 0.75V (see Figure 1).									
t _{PLH}	LOW to HIGH Propagation Delay	from (Input) SCL2 or SDA2	0	2.5	0	1.7	0	1.2	ns
t _{PHL}	HIGH to LOW Propagation Delay	to (Output) SCL1 or SDA1.	0	3.0	0	2.0	0	1.3	ns

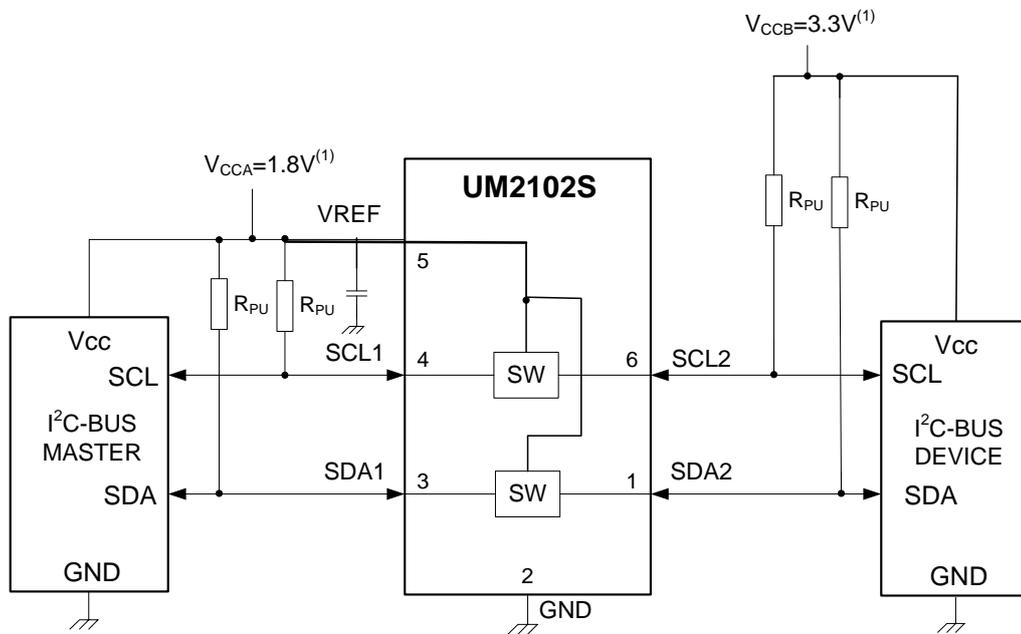
Switching Characteristics (Translating Up)

Over recommended operating free-air temperature range (unless otherwise noted). Values guaranteed by design.

Symbol	Parameter	Test Conditions	C _L =50pF		C _L =30pF		C _L =15pF		Unit
			Min	Max	Min	Max	Min	Max	
V _{REF} = 2.3V; V _{IH} = 2.3V; V _{IL} = 0V; V _{TI} = 3.3V; V _M = 1.15V ; R _L = 300 Ω (see Figure 1).									
t _{PLH}	LOW to HIGH Propagation Delay	from (Input) SCL1 or SDA1	0	2.35	0	1.5	0	1.0	ns
t _{PHL}	HIGH to LOW Propagation Delay	to (Output) SCL2 or SDA2.	0	3.35	0	2.25	0	1.4	ns
V _{REF} = 1.5V; V _{IH} = 1.5V; V _{IL} = 0V; V _{TI} = 2.5V; V _M = 0.75V ; R _L = 300 Ω (see Figure 1).									
t _{PLH}	LOW to HIGH Propagation Delay	from (Input) SCL1 or SDA1	0	2.35	0	1.5	0	1.0	ns
t _{PHL}	HIGH to LOW Propagation Delay	to (Output) SCL2 or SDA2.	0	3.5	0	2.5	0	1.5	ns



Typical Application Circuit



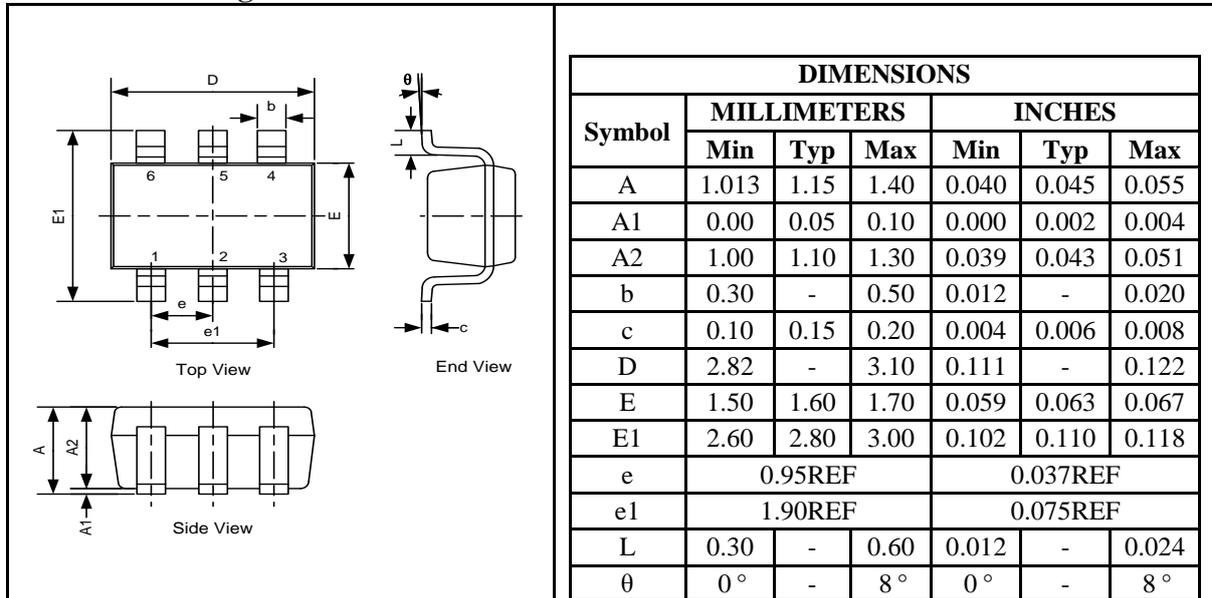
(1) The applied voltages at V_{CCA} and V_{CCB} should be such that V_{CCB} is at least 1 V higher than V_{CCA} for best translator operation.

Figure 2. Typical application circuit (switch always enabled)

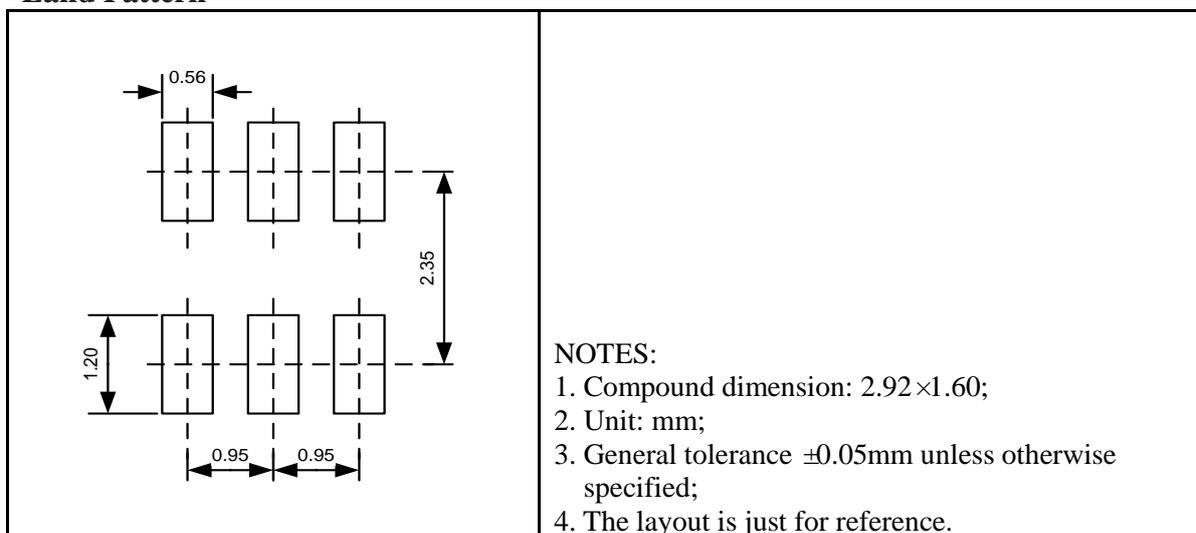
Package Information

SOT23-6

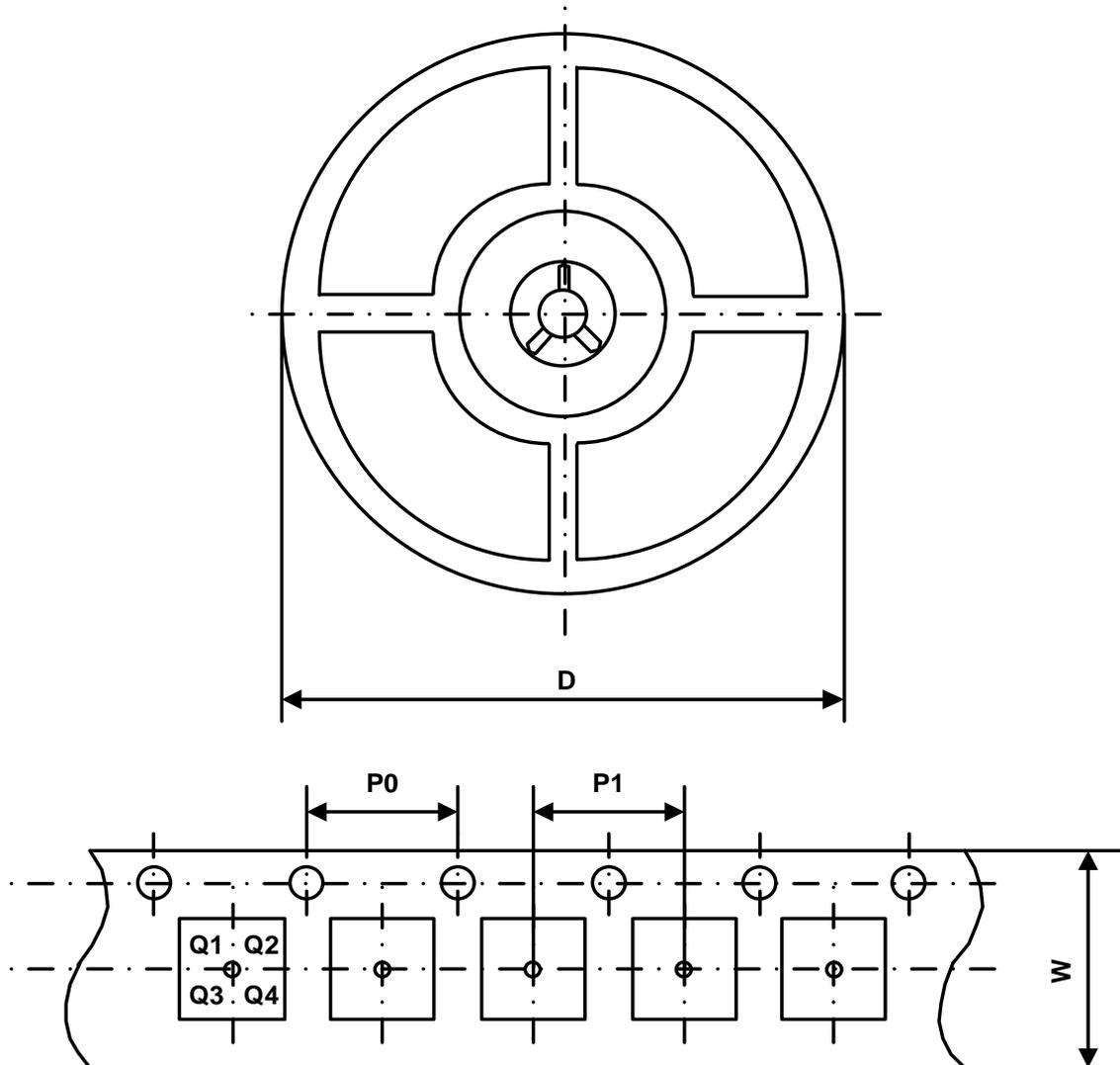
Outline Drawing



Land Pattern



Packing Information



Part Number	Package Type	Carrier Width (W)	Pitch (P0)	Pitch (P1)	Reel Size (D)	PIN 1 Quadrant
UM2102S	SOT23-6	8 mm	4 mm	4 mm	180 mm	Q3

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