

用于开漏和推挽应用的双向电压电平转换器

UM2002S8 SOP8
UM2002U8 TSSOP8

描述

UM2002 是双向电压电平转换器，工作电压范围为 1.0V 至 3.6V ($V_{\text{ref(A)}}$) 和 1.8V 至 5.5V ($V_{\text{ref(B)}}$)，可在开漏或推挽应用中进行 1.0V 和 5.0V 之间的双向电压转换而无需方向引脚。对于具有 50pF 电容和 197 Ω 上拉电阻的开漏系统，可为传输速度<33MHz 的电平转换应用提供 1 位或 2 位的位宽。

UM2002 可为低电压器件提供出色的 ESD 保护，同时还能保护抗 ESD 能力较弱的器件。

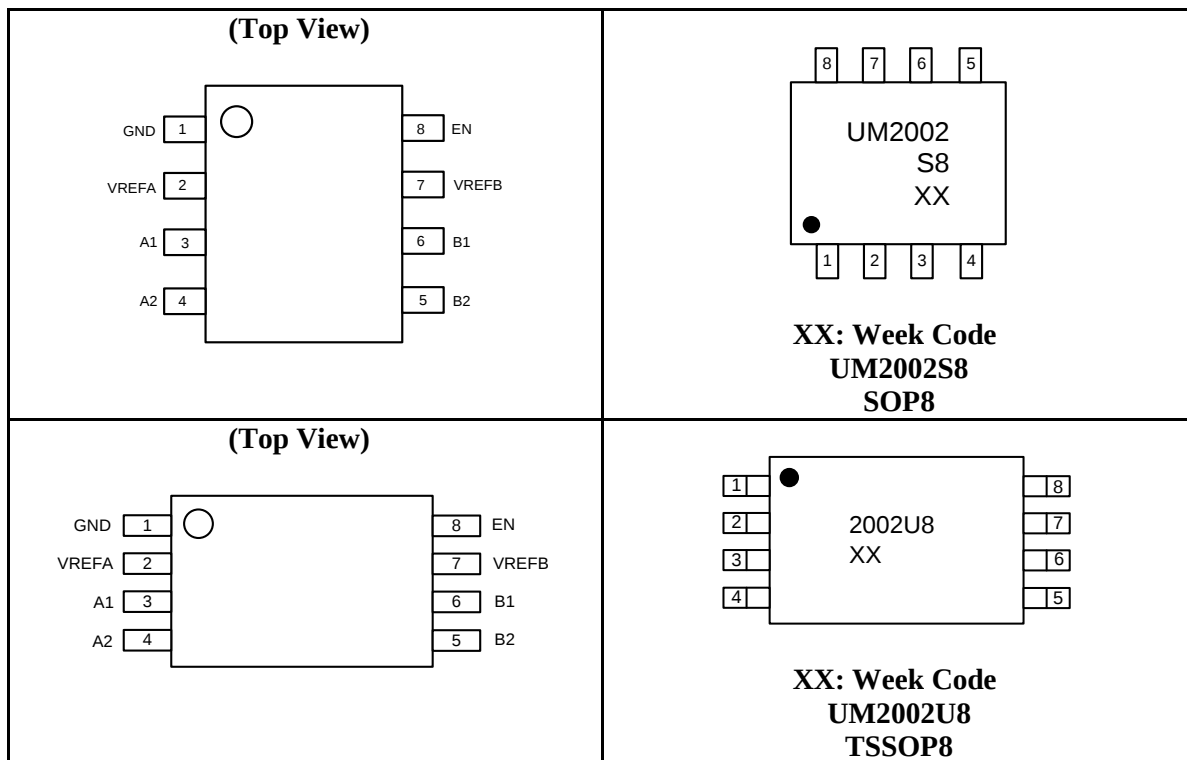
应用

特性

- SPI, MICROWIRE 和 I²C 电平转换
- 低压 ASIC 电平转换
- 智能读卡器
- 手机支架
- 便携式 POS 系统
- 便携式通信设备
- 低成本串行接口
- 蜂窝电话
- GPS
- 通信设备
- 消费类电子产品
- 家用电器
- 提供双向电压转换，无方向引脚
- 低于 1.5ns 的最大传输延迟
- 允许以下电压之间的电压电平转换：
 - 1.0V $V_{\text{ref(A)}}$ 和 1.8V, 2.5V, 3.3V 或 5V $V_{\text{ref(B)}}$
 - 1.2V $V_{\text{ref(A)}}$ 和 1.8V, 2.5V, 3.3V 或 5V $V_{\text{ref(B)}}$
 - 1.8V $V_{\text{ref(A)}}$ 和 3.3V 或 5V $V_{\text{ref(B)}}$
 - 2.0V $V_{\text{ref(A)}}$ 和 5V $V_{\text{ref(B)}}$
 - 3.3V $V_{\text{ref(A)}}$ 和 5V $V_{\text{ref(B)}}$
- 输出和输出端口之间的低至 3.5 Ω 的导通状态带来更少的信号失真
- 5V 耐压 I/O 端口，支持混合模式信号操作
- EN 为低电平时，An 和 Bn 引脚为高阻抗
- 无锁定操作
- 引脚排列便于印刷电路板走线
- ESD 保护：
 - 根据 JESD22-A114, HBM 超过 4000V
 - 根据 JESD22-A115, MM 超过 200V
 - 根据 JESD22-C101, CDM 超过 1000V
- 可用封装：SOP8、TSSOP8

Pin Configurations

Top View



Pin Description

Pin Number	Symbol	Function
1	GND	Ground (0V)
2	VREFA	Low-voltage side reference supply voltage for An
3,4	A1,A2	Low-voltage side; connected to VREFA through a pull-up resistor
5,6	B1,B2	High-voltage side; connected to VREFB through a pull-up resistor
7	VREFB	High-voltage side reference supply voltage for Bn
8	EN	Switch enable input; connected to VREFB and pulled-up through a high resistor

Ordering Information

Part Number	Packaging Type	Marking Code	Shipping Qty
UM2002S8	SOP8	UM2002S8	3000pcs/13Inch Tape & Reel
UM2002U8	TSSOP8	2002U8	3000pcs/13Inch Tape & Reel

Absolute Maximum Ratings (Note 1)

Over operating free-air temperature range (unless otherwise noted)

Symbol	Parameter		Value	Unit
$V_{ref(A)}$	Reference Voltage (A)		-0.5 to +6	V
$V_{ref(B)}$	Reference Voltage (B)		-0.5 to +6	V
V_I	Input Voltage		-0.5(Note 2) to +6	V
$V_{I/O}$	Voltage on an input/output pin		-0.5(Note 2) to +6	V
I_{ch}	Channel Current (DC)		+128	mA
I_{IK}	Input Clamp Current	$V_I < 0V$	-50	mA
T_{stg}	Storage Temperature		-65 to +150	°C

Note 1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Note 2: The input and input/output negative voltage ratings may be exceeded if the input and input/output clamp current ratings are observed.

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{I/O}$	Voltage on an input/output pin	An, Bn	0	5.5	V
$V_{ref(A)}$ (Note 3)	Reference Voltage (A)	VREFA	0	5.4	V
$V_{ref(B)}$ (Note 3)	Reference Voltage (B)	VREFB	0	5.5	V
$V_{I(EN)}$	Input Voltage on pin EN		0	5.5	V
$I_{sw(pass)}$	Pass Switch Current			64	mA
T_{amb}	Ambient Temperature	Operating in free-air	-40	+85	°C

Note 3: $V_{ref(A)} \leq V_{ref(B)} - 1V$ for best results in level shifting applications.

Electrical Characteristics

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ (Note 4)	Max	Unit
V_{IK}	Input Clamping Voltage	$I_I = -18\text{mA}$; $V_{I(EN)} = 0\text{V}$			-1.2	V
I_{IH}	HIGH-level Input Current	$V_I = 5\text{V}$; $V_{I(EN)} = 0\text{V}$			5	μA
$C_{i(EN)}$	Input Capacitance on pin EN	$V_I = 0\text{V}$ or 3V		12		pF
$C_{io(off)}$	Off-state input/output capacitance	An, Bn; $V_O = 0\text{V}$ or 3V ; $V_{I(EN)} = 0\text{V}$		10	12	pF
$C_{io(on)}$	On-state input/output capacitance	An, Bn; $V_O = 0\text{V}$ or 3V ; $V_{I(EN)} = 3\text{V}$		8	12.5 (Note 5)	pF
R_{on}	ON-state resistance (Note 6)	An, Bn; $V_I = 0\text{V}$; $I_O = 64\text{mA}$; $V_{I(EN)} = 4.5\text{V}$ (Note 7)	1	2.5	5.0	Ω
		An, Bn; $V_I = 2.4\text{V}$; $I_O = 15\text{mA}$; $V_{I(EN)} = 4.5\text{V}$		4.5	7.5	

Note 4: All typical values are at $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Note 5: Not production tested, maximum value based on characterization data of typical parts.

Note 6: Measured by the voltage drop between the An and Bn terminals at the indicated current through the switch. ON-state resistance is determined by the lowest voltage of the two terminals.

Note 7: Guaranteed by design.

Switching Characteristics (translating down)

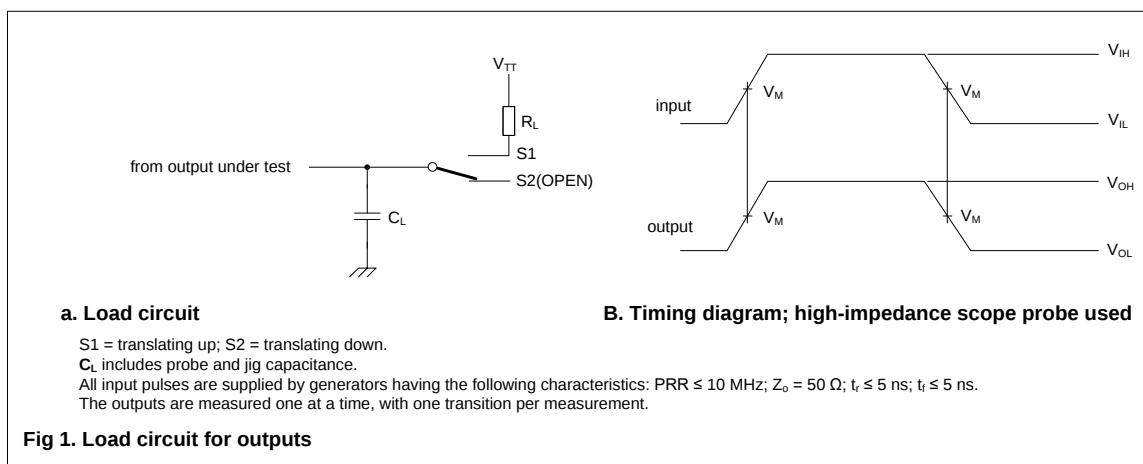
Over recommended operating free-air temperature range(unless otherwise noted). Values guaranteed by design.

Symbol	Parameter	Test Conditions	C _L =50pF		C _L =30pF		C _L =15pF		Unit
			Min	Max	Min	Max	Min	Max	
V _{I(EN)} = 3.3V; V _{IH} = 3.3V; V _{IL} = 0V; V _M = 1.15V(see Figure 1).									
t _{PLH}	LOW to HIGH propagation delay	from (input) Bn to (output) An.	0	3.5	0	2.7	0	2.2	ns
t _{PHL}	HIGH to LOW propagation delay		0	3.5	0	3.0	0	2.3	ns
V _{I(EN)} =2.5V; V _{IH} = 2.5V; V _{IL} = 0V; V _M = 0.75V (see Figure 1).									
t _{PLH}	LOW to HIGH propagation delay	from (input) Bn to (output) An.	0	3.5	0	2.7	0	2.2	ns
t _{PHL}	HIGH to LOW propagation delay		0	4.0	0	3.0	0	2.3	ns

Switching Characteristics (translating up)

Over recommended operating free-air temperature range(unless otherwise noted). Values guaranteed by design.

Symbol	Parameter	Test Conditions	C _L =50pF		C _L =30pF		C _L =15pF		Unit
			Min	Max	Min	Max	Min	Max	
V _{I(EN)} = 3.3V; V _{IH} = 2.3V; V _{IL} = 0V; V _{TT} = 3.3V; V _M = 1.15V; R _L = 300Ω(see Figure 1).									
t _{PLH}	LOW to HIGH propagation delay	from (input) An to (output) Bn.	0	3.35	0	2.5	0	2.0	ns
t _{PHL}	HIGH to LOW propagation delay		0	4.35	0	3.25	0	2.4	ns
V _{I(EN)} =2.5V; V _{IH} = 1.5V; V _{IL} = 0V; V _{TT} = 2.5V; V _M = 0.75V; R _L = 300Ω (see Figure 1).									
t _{PLH}	LOW to HIGH propagation delay	from (input) An to (output) Bn.	0	3.35	0	2.5	0	2.0	ns
t _{PHL}	HIGH to LOW propagation delay		0	4.5	0	3.5	0	2.5	ns



Applications Information

Detail Description

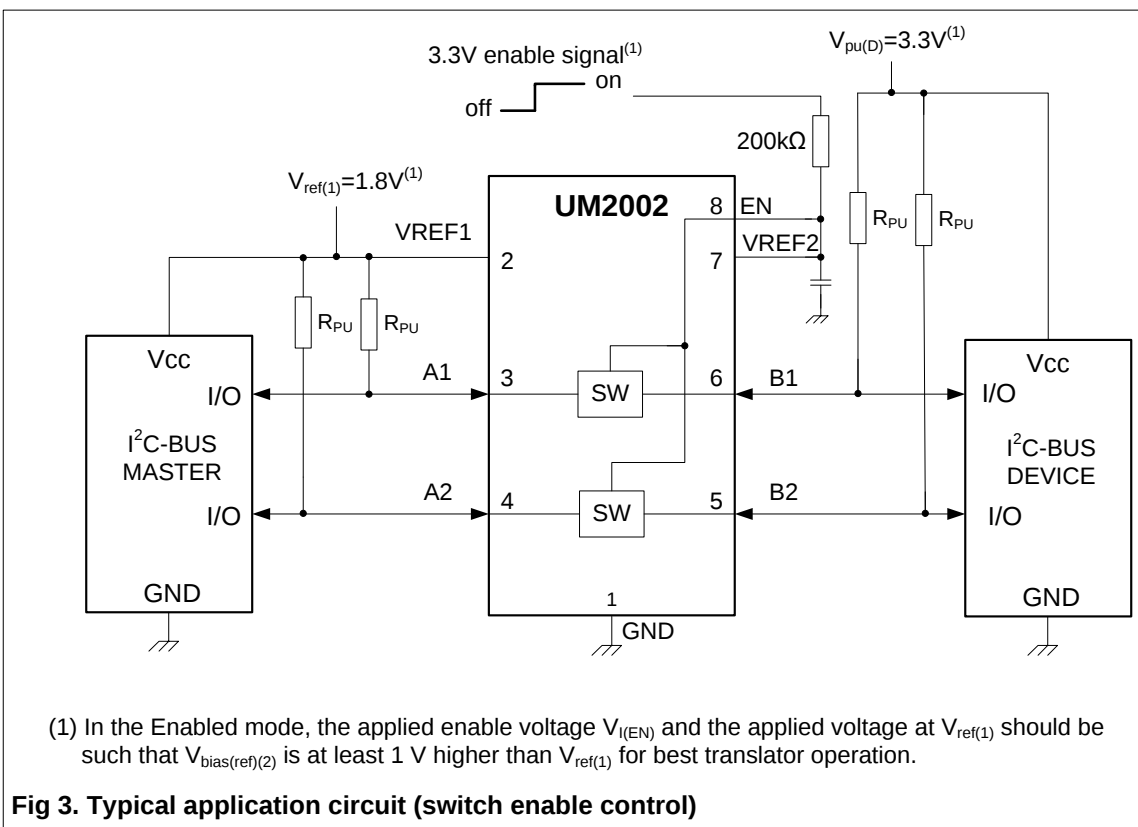
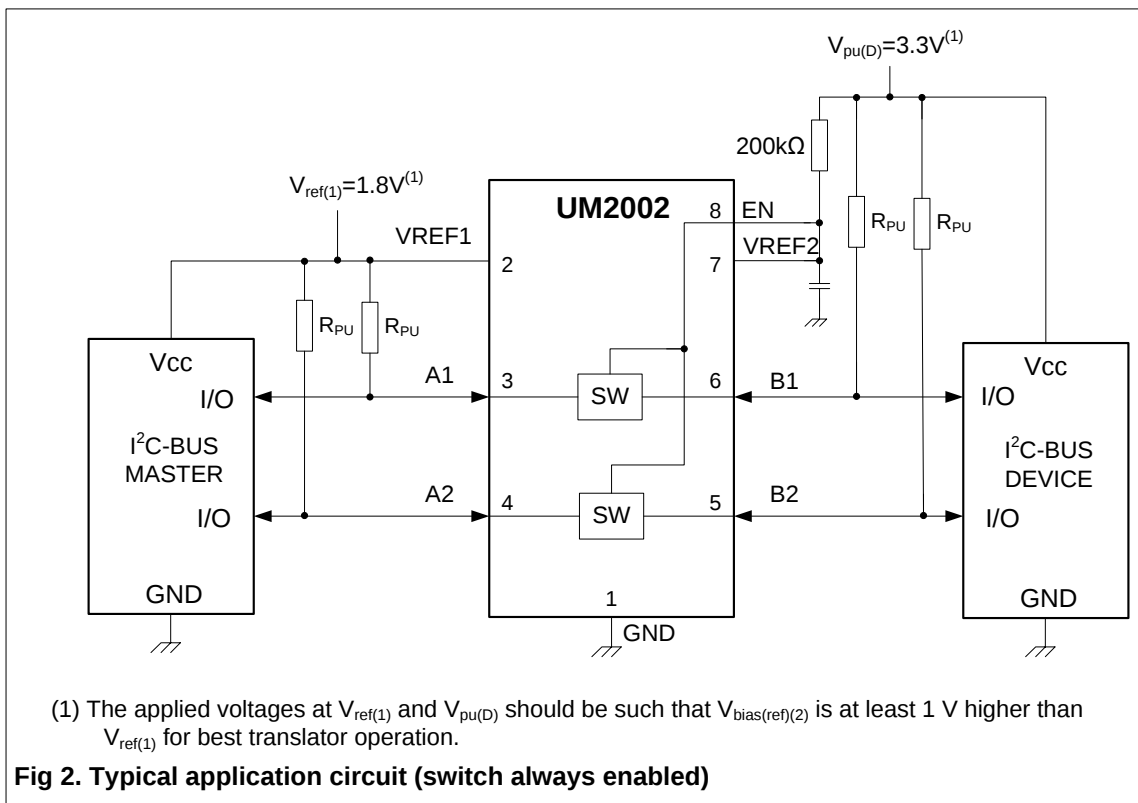
The UM2002 is a bidirectional voltage level translator operational from 1.0V to 3.6V ($V_{ref(A)}$) and 1.8V to 5.5V ($V_{ref(B)}$), which allows bidirectional voltage translations between 1.0V and 5V without the need for a direction pin in open-drain or push-pull applications.

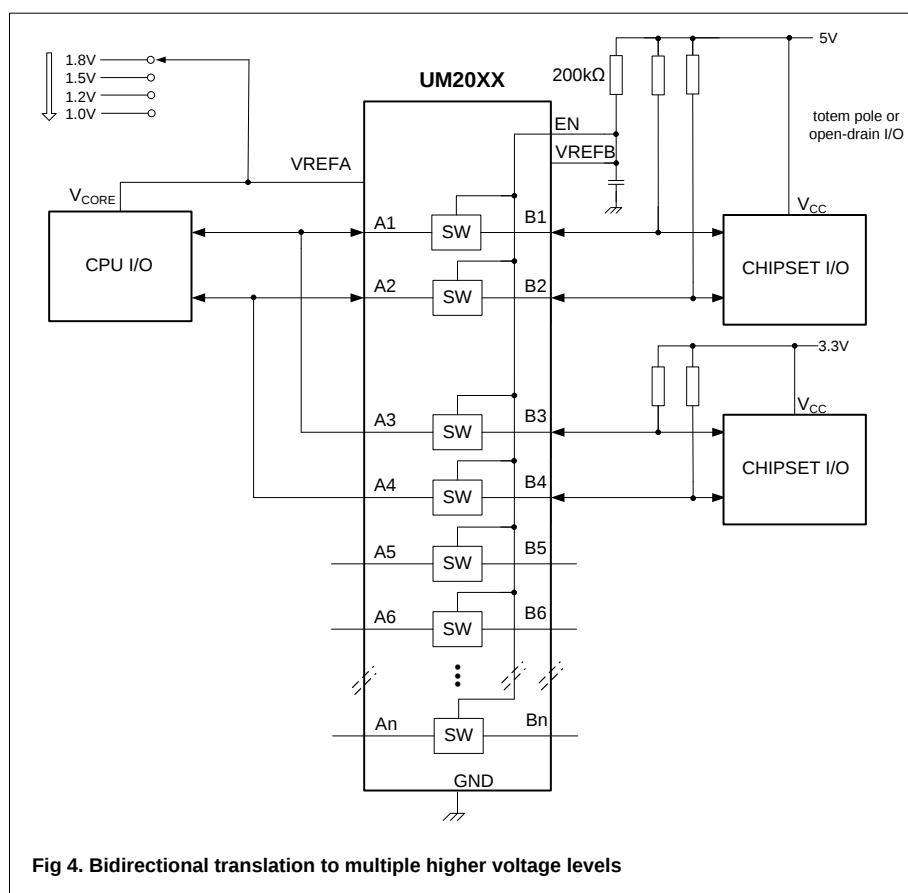
When the An or Bn port is LOW, the clamp is in the ON-state and a low resistance connection exists between the An and Bn ports. The low ON-state resistance (R_{on}) of the switch allows connections to be made with minimal propagation delay. Assuming the higher voltage is on the Bn port when the Bn port is HIGH, the voltage on the An port is limited to the voltage set by $V_{ref(A)}$. When the An port is HIGH, the Bn port is pulled to the drain pull-up supply voltage ($V_{pu(D)}$) by the pull-up resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user without the need for directional control.

When EN is HIGH, the translator switch is on, and the An I/O are connected to the Bn I/O, respectively, allowing bidirectional data flow between ports. When EN is LOW, the translator switch is off, and a high-impedance state exists between ports. The EN input circuit is designed to be supplied by $V_{ref(B)}$. To ensure the high-impedance state during power-up or power-down, EN must be LOW.

All channels have the same electrical characteristics and there is minimal deviation from one output to another in voltage or propagation delay. This is a benefit over discrete transistor voltage translation solutions, since the fabrication of the switch is symmetrical.

Enable and Disable





Bidirectional translation

For the bidirectional clamping configuration (higher voltage to lower voltage or lower voltage to higher voltage), the EN input must be connected to VREFB and both pins pulled to HIGH side $V_{pu(D)}$ through a pull-up resistor (typically 200k Ω). This allows VREFB to regulate the EN input. A filter capacitor on VREFB is recommended. The master output driver can be totem pole or open-drain (pull-up resistors may be required) and the slave device output can be totem pole or open-drain (pull-up resistors are required to pull the Bn outputs to $V_{pu(D)}$). However, if either output is totem pole, data must be unidirectional or the outputs must be 3-stateable and be controlled by some direction-control mechanism to prevent HIGH-to-LOW contentions in either direction. If both outputs are open-drain, no direction control is needed.

The reference supply voltage ($V_{\text{ref(A)}}$) is connected to the processor core power supply voltage. When VREFB is connected through a 200k Ω resistor to a 3.3V to 5.5V $V_{\text{pu(D)}}$ power supply, and $V_{\text{ref(A)}}$ is set between 1.0V and ($V_{\text{pu(D)}} - 1V$), the output of each An has a maximum output voltage equal to VREFA, and the output of each Bn has a maximum output voltage equal to $V_{\text{pu(D)}}$.

Application operating conditions

Refer to Figure 4

Symbol	Parameter	Conditions	Min	Typ (Note 8)	Max	Unit
$V_{ref(B)}$	Reference Bias Voltage (B)		$V_{ref(A)} + 0.6$	2.1	5	V
$V_{I(EN)}$	Input Voltage on pin EN		$V_{ref(A)} + 0.6$	2.1	5	V
$V_{ref(A)}$	Reference Voltage (A)		0	1.5	4.4	V
$I_{sw(pass)}$	Pass Switch Current			14		mA
I_{ref}	Reference Current	Transistor		5		μA
T_{amb}	Ambient Temperature	Operating in free-air	-40		+85	$^{\circ}C$

Note 8: All typical values are at $T_{amb} = 25^{\circ}C$.

Sizing pull-up resistor

The pull-up resistor value needs to limit the current through the pass transistor when it is in the ON state to about 15mA. This ensures a pass voltage of 260mV to 350mV. If the current through the pass transistor is higher than 15mA, the pass voltage also is higher in the ON state. To set the current through each pass transistor at 15mA, the pull-up resistor value is calculated as:

$$R_{PU} = \frac{V_{pu(D)} - 0.35V}{0.015 A}$$

The table below summarizes resistor reference voltages and currents at 15mA, 10mA, and 3mA. The resistor values shown in the +10 % column or a larger value should be used to ensure that the pass voltage of the transistor would be 350 mV or less. The external driver must be able to sink the total current from the resistors on both sides of the UM2002 device at 0.175V, although the 15mA only applies to current flowing through the UM2002 device.

Pull-up resistor values

Calculated for $V_{OL} = 0.35V$; assumes output driver $V_{OL} = 0.175V$ at stated current.

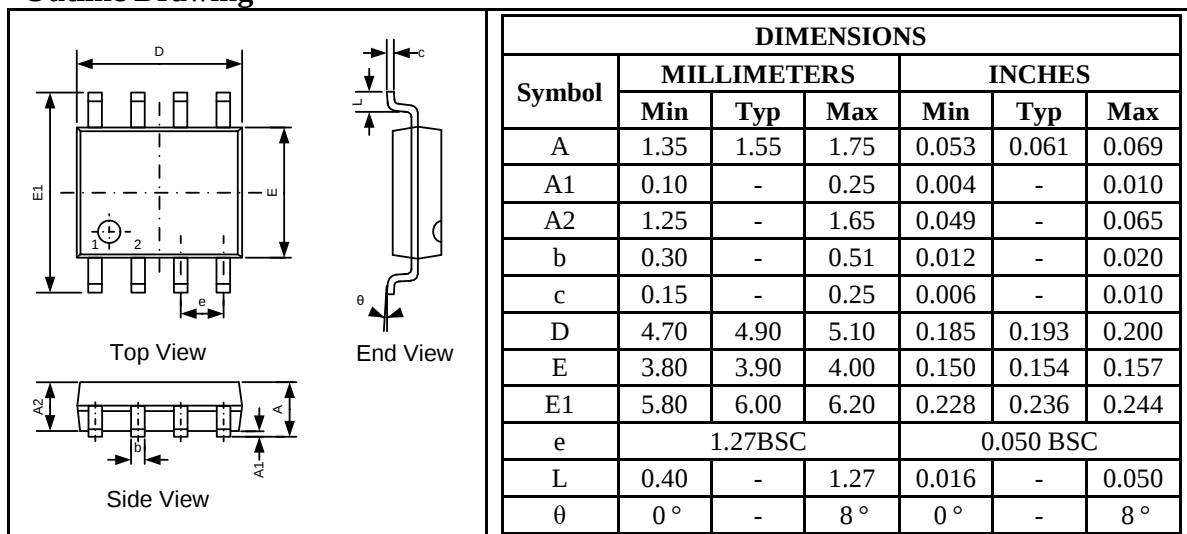
$V_{pu(D)}$	Pull-up resistor value (Ω)					
	15mA		10mA		3mA	
	Nominal	+10 % (Note 9)	Nominal	+10 % (Note 9)	Nominal	+10 % (Note 9)
5V	310	341	465	512	1550	1705
3.3V	197	217	295	325	983	1082
2.5V	143	158	215	237	717	788
1.8V	97	106	145	160	483	532
1.5V	77	85	115	127	383	422
1.2V	57	63	85	94	283	312

Note 9: +10 % to compensate for V_{CC} range and resistor tolerance.

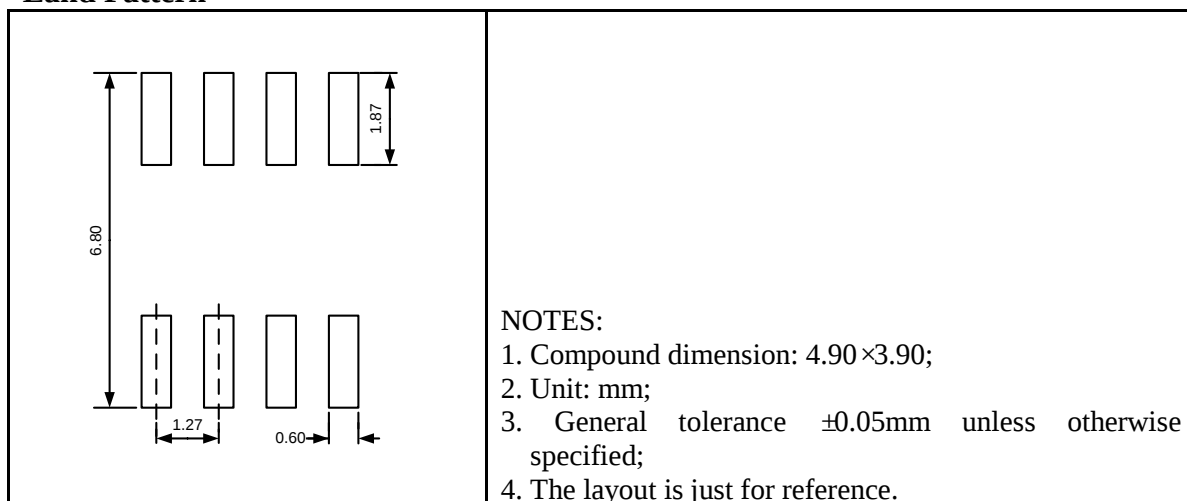
Package Information

UM2002S8 SOP8

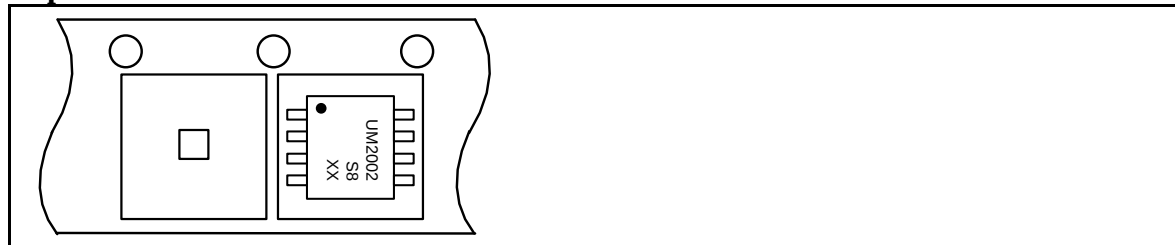
Outline Drawing



Land Pattern

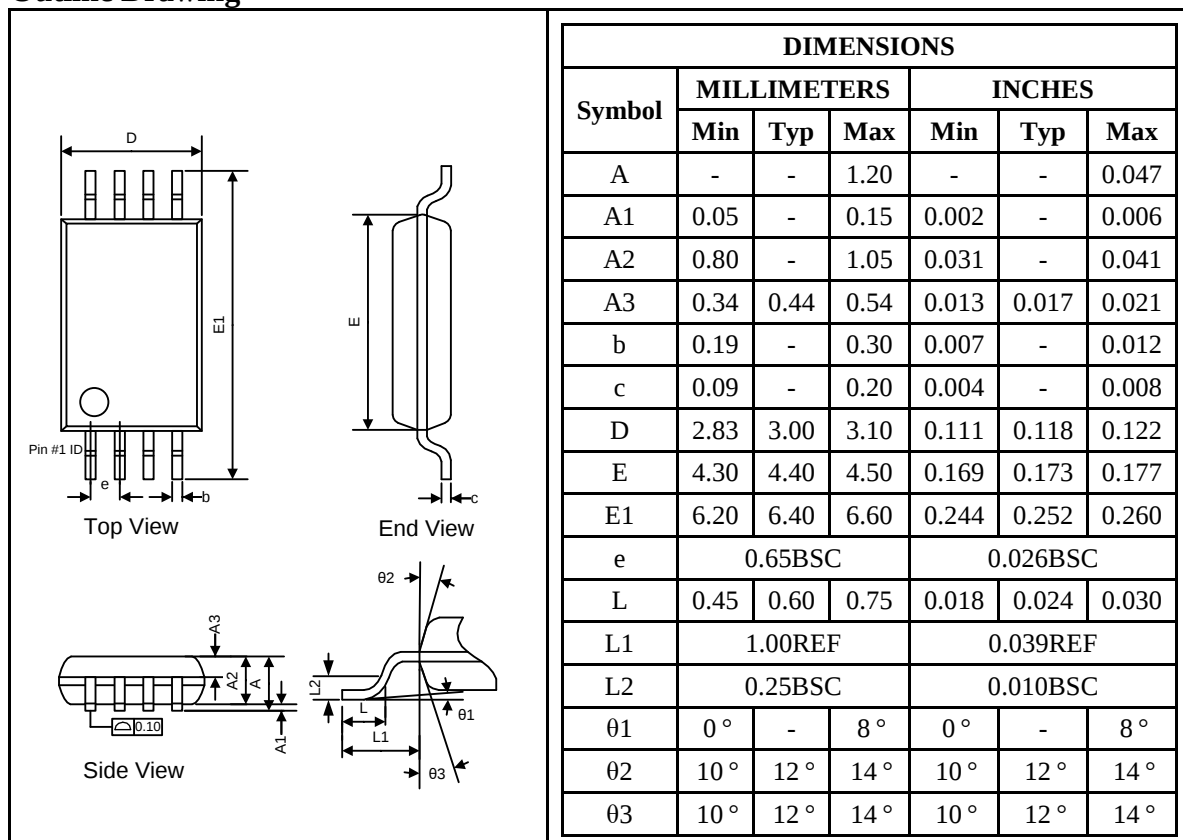


Tape and Reel Orientation

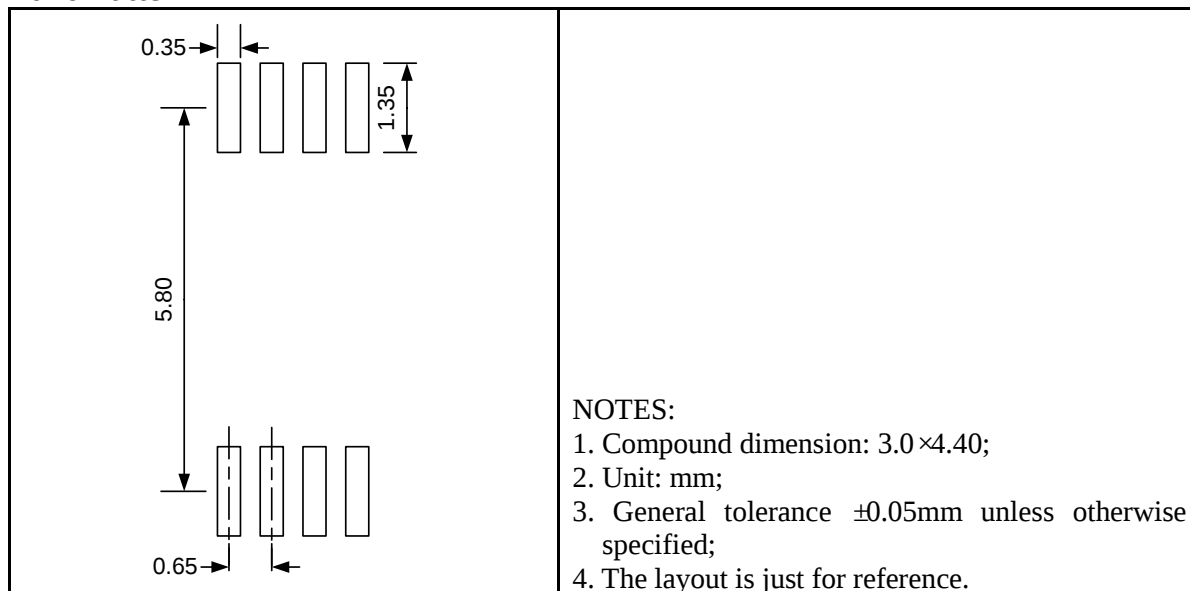


UM2002U8: TSSOP8

Outline Drawing



Land Pattern



Tape and Reel Orientation



GREEN COMPLIANCE

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