

双通道ESD保护设备

UM1001 SOT23-6

描述

UM1001是一款集成 TVS 二极管的低通滤波器阵列，用于ESD保护。该器件专为便携式电子设备设计，可提供对电磁干扰（EMI）/射频干扰（RFI）信号的单向滤波以及静电放电（ESD）保护。这款先进的器件采用固态硅雪崩技术，可实现优异的箝位性能和直流电气特性。该器件已针对手机及其他便携式电子设备的 USB 接口进行了优化。

UM1001 通过将10个离散组件集成于小型SOT23-6封装中，实现ESD保护与EMI滤波功能。该小型封装可保护并滤波多达两条线路。其紧凑的封装设计使其特别适用于便携式应用。

TVS 二极管为单向结构，可支持无失真的单极性信号。TVS二极管可有效抑制超过 $\pm 15\text{kV}$ （空气间隙放电）和 $\pm 8\text{kV}$ （接触放电）的ESD电压，符合IEC 61000-4-2标准的第4级要求。该器件在通带内（约为 10MHz）插入损耗非常低，且在 800MHz 至 3GHz 频率范围内具有高衰减特性。每条线路均配备两级TVS二极管保护。该器件采用大截面积结点以导通高瞬态电流，且具备电路板级保护的理理想特性，包括快速响应时间、低工作电压和钳位电压，以及无器件退化。

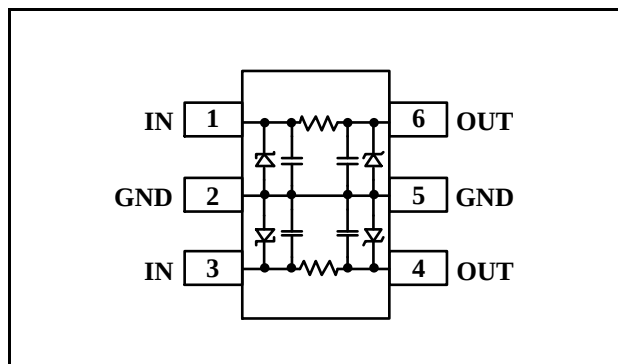
应用

- 网络平板电脑和手持设备
- 笔记本
- 便携式设备
- 工业接口
- 跑步机

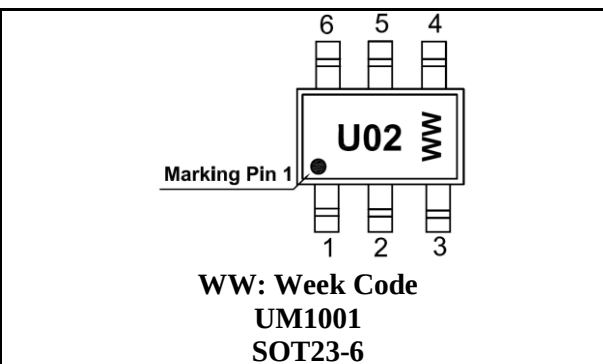
特性

- 数据线瞬态保护，符合IEC 61000-4-2标准： $\pm 15\text{kV}$ （空气间隙放电）和 $\pm 8\text{kV}$ （接触放电）
- 集成 ESD 保护功能的单向 EMI/RFI 滤波器
- 可保护两条I/O线路
- 反向工作电压：5V
- 低漏电流
- 低工作电压和钳位电压
- 采用固态硅雪崩技术

引脚配置



顶部视图



Ordering Information

Part Number	Working Voltage	Packaging Type	Channel	Marking Code	Shipping Qty
UM1001	5.0V	SOT23-6	2	U02	3000pcs/7Inch Tape & Reel

Absolute Maximum Ratings

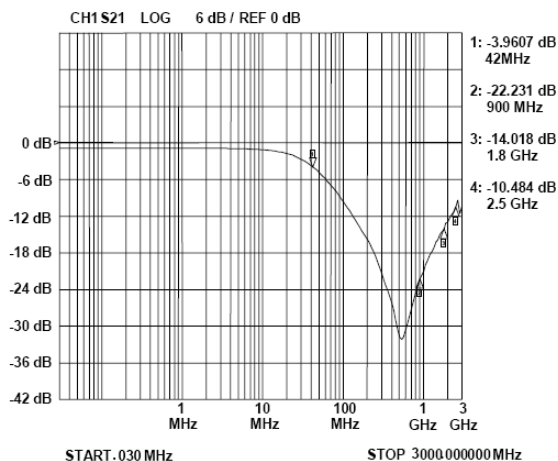
Rating	Symbol	Value	Unit
Steady-State Power	P_{SS}	100	mW
Junction Temperature	T_J	-40 to +125	℃
Operating Temperature	T_{OP}	-40 to +85	℃
Storage Temperature	T_{STG}	-55 to +150	℃

Electrical Characteristics (T=25 ℃)

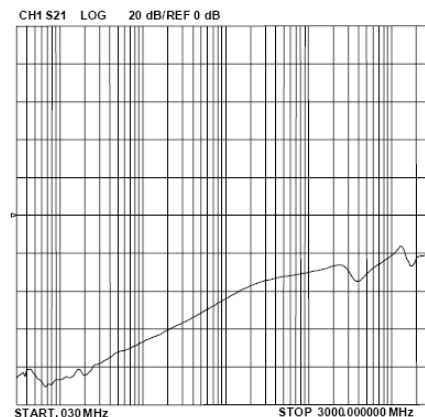
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Stand-Off Voltage	V_{RWM}				5	V
Reverse Breakdown Voltage	V_{BR}	$I_T=1mA$	6			V
Reverse Leakage Current	I_R	$V_{RWM}=5V, T=25\text{ }^{\circ}\text{C}$			5	μA
Series Resistance	R	Each Line		10		Ω
Total Capacitance	C_{TOT}	Any I/O to GND $V_R=0V, f=1MHz$			20	pF

Typical Operating Characteristics

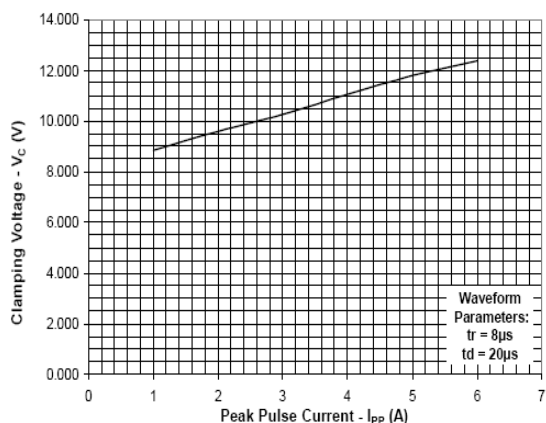
Typical Insertion Loss



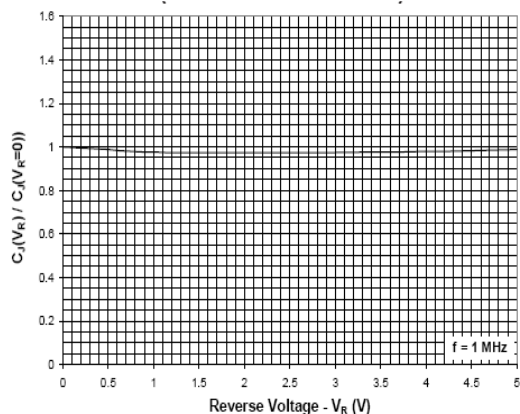
Analog Crosstalk



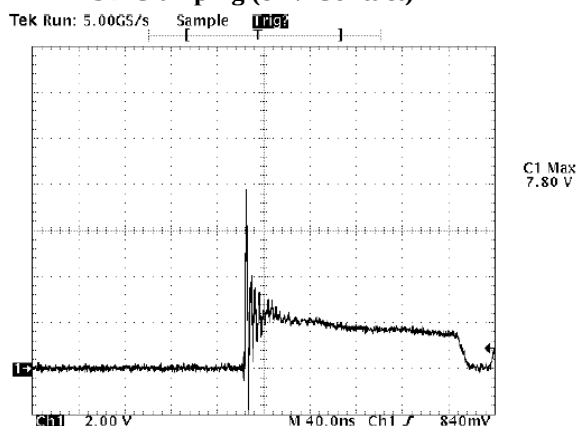
Forward Voltage vs. Peaking Pulse Current



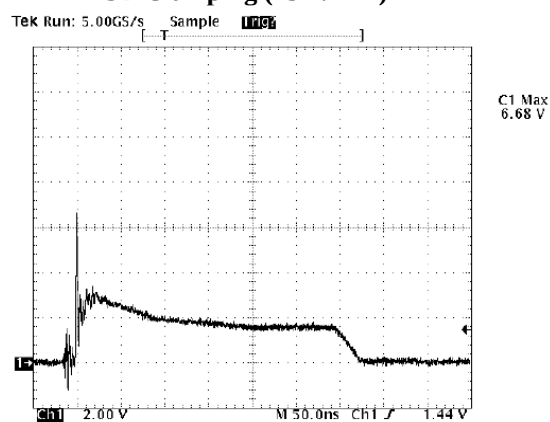
Junction Capacitance vs. Reverse Voltage



ESD Clamping (8kV Contact)



ESD Clamping (15kV Air)



Application Information

Device Connection for Protection of Quad Data Lines

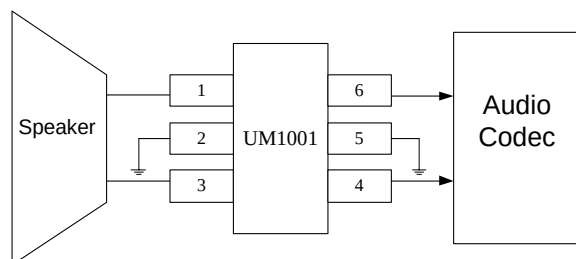
The UM1001 provides EMI filtering and ESD protection in a small SOT23-6 package for dual line data port applications. The layout of the device is designed such that the data lines can be routed through the device. The first line pair enters at pin 1 and exits at pin 6. The second line pair enters at pin 3 and exits at pin 4. The device is symmetrical so the above connections may be reversed.

Circuit Board Layout Recommendations for Suppression of ESD

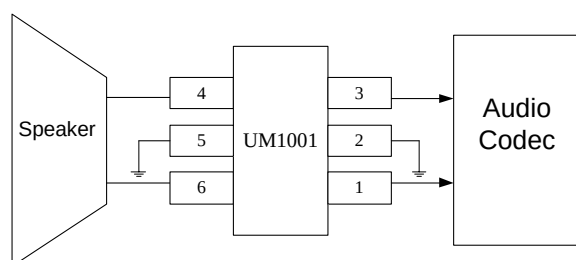
Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

1. Place the TVS near the input terminals or connectors to restrict transient coupling.
2. Minimize the path length between the TVS and the protected line.
3. Minimize all conductive loops including power and ground loops.
4. The ESD transient return path to ground should be kept as short as possible.
5. Never run critical signals near board edges.
6. Use ground planes whenever possible.

Layout Example



Pin	Identification
1	Line 1 In (From Speaker)
6	Line 1 Out (To Audio Circuit)
3	Line 2 In (From Speaker)
4	Line 2 Out (To Audio Circuit)
2, 5	Ground

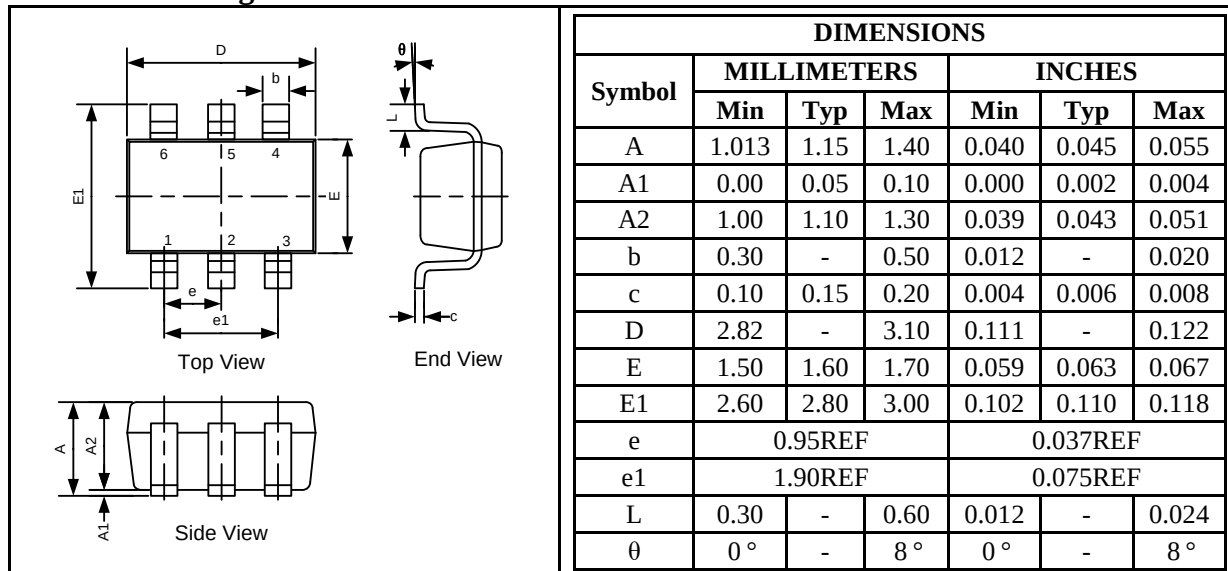


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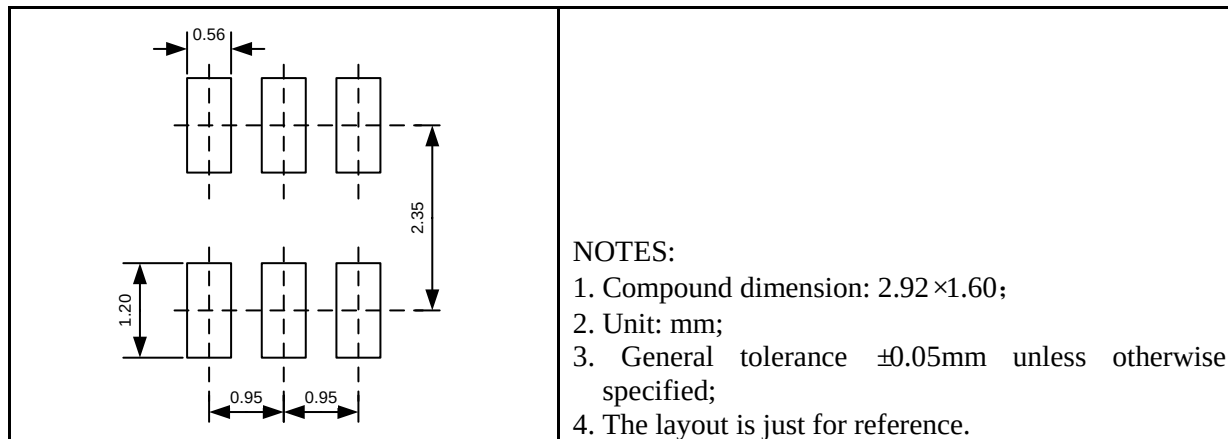
Package Information

UM1001 SOT23-6

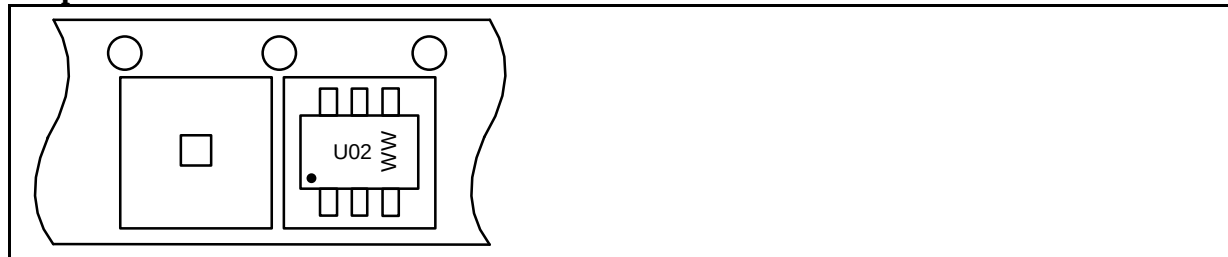
Outline Drawing



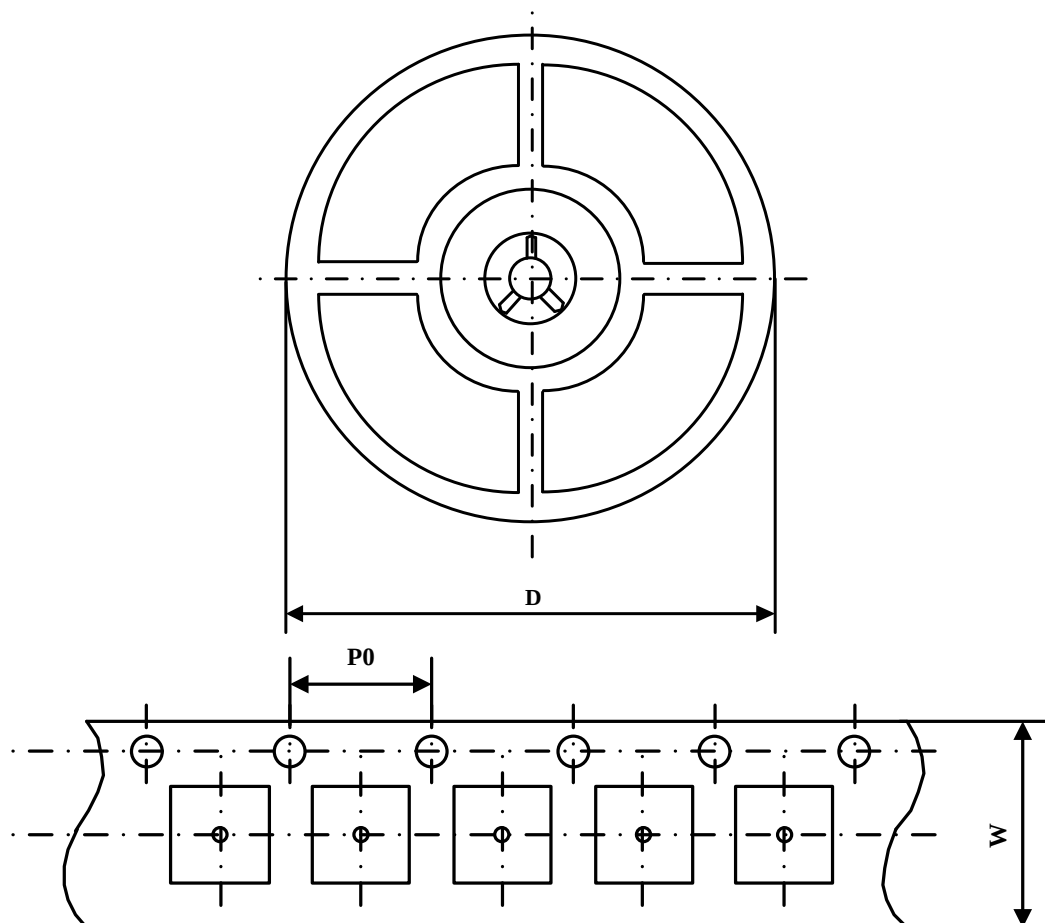
Land Pattern



Tape and Reel Orientation



Packing Information



Part Number	Package Type	Carrier Width(W)	Pitch(P0)	Reel Size(D)
UM1001	SOT23-6	8 mm	4 mm	180 mm

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