

双通道ESD保护二极管阵列 UESD6V8S2B SOT523

描述

UESD6V8S2B TVS二极管阵列设计用于保护敏感元器件免于ESD 损坏或闩锁,适用于电路板空间有限的应用场合。该器件是单向设备,可用于信号极性高于地面的线路,每个器件最多可保护两条线路。

TVS 二极管是一种固态设备,具有大截面积结,可传导高瞬态电流,特别适用于瞬态抑制。 具有适用于板级电路保护的理想电气特性,包括快速响应时间、低工作电压、低钳位电压 和无器件劣化。

UESD6V8S2B可耐受符合IEC 61000-4-2标准的±15kV 空气间隙放电和±8kV 接触放电,以及MIL-STD-883 METHOD 3015标准的±8 kV HBM的抗扰度要求。其小型封装使其非常适合用于手机、PDA、笔记本电脑和数码相机等便携式电子产品。

应用

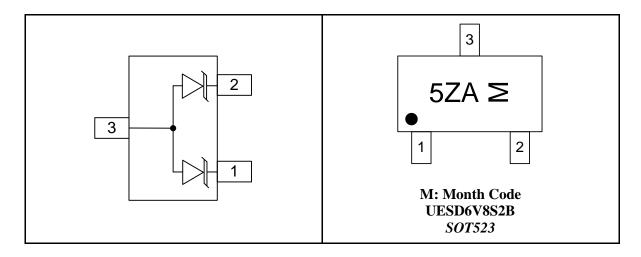
- 手机听筒和配件
- 无线电话
- PDA
- 笔记本电脑和掌上电脑
- 便携式设备
- 数码相机
- 外围设备
- MP3 播放器

特性

- 数据线和电源线瞬态保护,符合IEC 61000-4-2标准:±15kV(空气),±8kV(接触)
- 符合MIL-STD-883 3015 (HBM)标准: ±8kV
- 可保护两条I/O线
- 反向工作电压: 5V
- 低漏电电流
- 低工作电压和钳位电压
- 固态硅雪崩技术

引脚配置

顶部视图





Ordering Information

| Part Number | Working Voltage | Packaging Type | Channel | Marking Code | Shipping Qty |
|-------------|--------------------|----------------|---------|-----------------|------------------------------|
| UESD6V8S2B | 5.0V | SOT523 | 2 | 5ZA | 3000pcs/7Inch Tape & Reel |

Absolute Maximum Ratings

| Rating | Symbol | Value | Unit |
|---|------------|---------------|----------------|
| Peak Pulse Power (t _P =8/20μs) | P_{PK} | 140 | Watts |
| Peak Pulse Current (t _P =8/20μs) | I_{PP} | 11 | A |
| Lead Soldering Temperature | $T_{ m L}$ | 260 (10 sec.) | $\mathcal C$ |
| Operating Temperature | T_{J} | -55 to +125 | ${\mathcal C}$ |
| Storage Temperature | T_{STG} | -55 to +125 | ${\mathcal C}$ |

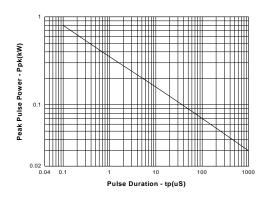
Electrical Characteristics

| Parameter | Symbol | Conditions | Min | Тур | Max | Unit |
|-------------------------------|----------------------|---|-----|-----|-----|------|
| Reverse Stand-Off Voltage | $V_{\rm RWM}$ | | | | 5 | V |
| Reverse Breakdown Voltage | V_{BR} | I _T =1mA | 6 | 6.8 | 7.2 | V |
| Reverse Leakage Current | I_R | $V_{RWM}=5V$, $T=25$ °C | | | 0.1 | μΑ |
| Clause Walter | $V_{\rm C}$ | $I_{PP}=5A, t_P=8/20\mu s$ | 9.1 | | 9.1 | V |
| Clamping Voltage | | $I_{PP}=11A$, $t_P=8/20\mu s$ | | | 13 | l v |
| Junction Capacitance | C_{J} | Pin 1, 2 to 3 V _R =0V, f=1MHz | | 40 | 50 | pF |
| Junction Capacitance | C_{J} | Pin 1, 2 to 3 V _R =2.5V, f=1MHz | | 30 | 40 | pF |
| Reverse Dynamic Resistance | $R_{\text{dyn,rev}}$ | I1 A 5 A | | 0.6 | | Ω |
| Forward Dynamic Resistance | $R_{dyn,fwd} \\$ | I _{PP} =1A~5A | | 0.5 | | Ω |

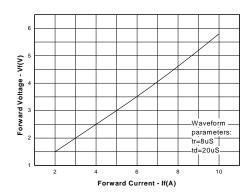
UESD6V8S2B

Typical Operating Characteristics

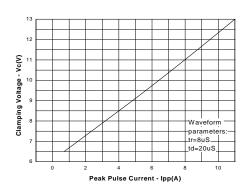
Non-Repetitive Peak Pulse Power vs. Pulse Time



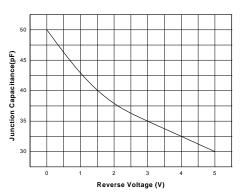
Forward Voltage vs. Forward Current



Clamping Voltage vs. Peak Pulse Current



Junction Capacitance vs. Reverse Voltage





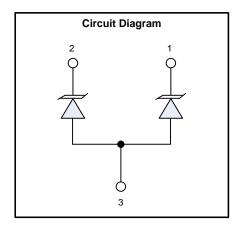
Applications Information

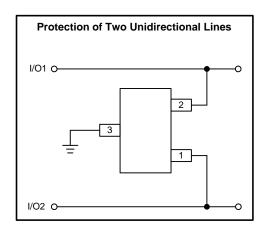
UESD6V8S2B ESD protection diode is designed to protect dual data, I/O, or power supply line. The device is unidirectional and may be used on lines where the signal polarity is above ground. The cathode should be placed towards the line that is to be protected.

Device Connection for Protection of Dual Data Lines

The Dual TVS Diode Array is designed to protect up to two unidirectional data lines. The device is connected as follows:

Unidirectional protection of two I/O lines is achieved by connecting pins 1 and 2 to the data lines. Pin 3 is connected to ground. The ground connection should be made directly to the ground plane for best results. The path length is kept as short as possible to reduce the effects of parasitic inductance in the board traces.





Circuit Board Layout Recommendations for Suppression of ESD

Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

Place the TVS near the input terminals or connectors to restrict transient coupling.

Minimize the path length between the TVS and the protected line.

Minimize all conductive loops including power and ground loops.

The ESD transient return path to ground should be kept as short as possible.

Never run critical signals near board edges.

Use ground planes whenever possible. For multilayer printed-circuit boards, use ground vias.

Keep parallel signal paths to a minimum.

Avoid running protection conductors in parallel with unprotected conductor.

Minimize all printed-circuit board conductive loops including power and ground loops.

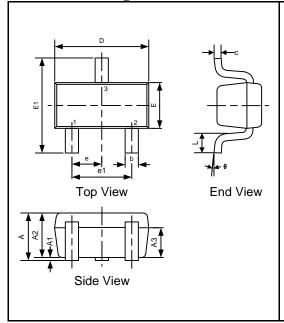
Avoid using shared transient return paths to a common ground point.



Package Information

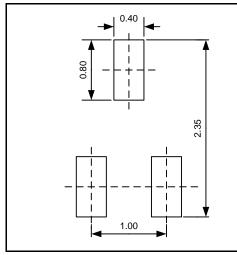
UESD6V8S2B SOT523

Outline Drawing



| DIMENSIONS | | | | | | | |
|------------|-------------|------|------|----------|-------|-------|--|
| Symbol | MILLIMETERS | | | INCHES | | | |
| | Min | Тур | Max | Min | Тур | Max | |
| A | 0.60 | 0.80 | 0.90 | 0.024 | 0.031 | 0.035 | |
| A1 | 0.00 | 0.05 | 0.10 | 0.000 | 0.002 | 0.004 | |
| A2 | 0.60 | 0.75 | 0.80 | 0.024 | 0.030 | 0.031 | |
| A3 | 0.45 | 0.50 | 0.65 | 0.018 | 0.020 | 0.026 | |
| b | 0.15 | 0.22 | 0.30 | 0.006 | 0.009 | 0.012 | |
| с | 0.10 | 0.12 | 0.20 | 0.004 | 0.005 | 0.008 | |
| D | 1.50 | 1.60 | 1.70 | 0.059 | 0.063 | 0.067 | |
| Е | 0.75 | 0.80 | 0.85 | 0.030 | 0.031 | 0.033 | |
| E1 | 1.45 | 1.60 | 1.75 | 0.057 | 0.063 | 0.069 | |
| e | 0.50TYP | | | 0.020TYP | | | |
| e1 | 0.90 | 1.00 | 1.10 | 0.035 | 0.039 | 0.043 | |
| L | 0.20 | 0.33 | 0.40 | 0.008 | 0.013 | 0.016 | |
| θ | 0° | - | 8° | 0 ° | - | 8° | |

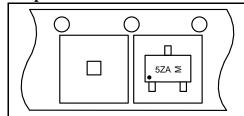
Land Pattern



NOTES:

- 1. Compound dimension: 1.60×0.80;
- 2. Unit: mm;
- 3. General tolerance ±0.05mm unless otherwise specified;
- 4. The layout is just for reference.

Tape and Reel Orientation





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http://www.union-ic.com/index.aspx?cat_code=RoHSDeclaration

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