

## 低电容、单通道ESD保护二极管

#### UESD6V8L1F DFN2 1.0×0.6

#### 描述

UESD6V8L1F 是一款ESD保护二极管,专为替代便携式应用(如手机、笔记本电脑和PDA)中的多层压敏电阻(MLVs)而设计。与多层变阻器相比,它们具有可传导高瞬态电流的大横截面积结点,可为板级保护提供理想的电气特性,如快速响应时间、较低的工作电压、较低的箝位电压和无器件劣化。

UESD6V8L1F ESD保护二极管可保护敏感的半导体元件免受静电放电 (ESD) 和其他电压诱导瞬态事件造成的损坏或破坏。UESD6V8L1F采用DFN2 1.0×0.6(与SOD882兼容)封装,工作电压为5 V。

在不适合采用阵列的应用中,设计人员可以采用该器件灵活地保护一条单向线路。此外,在电路板空间有限的应用中,它还可以"散布"在电路板周围。该器件可耐受±15kV的空气放电和±8kV的接触放电,符合IEC 61000-4-2标准第4级要求。

UESD6V8L1F 采用双扩散技术制造,具有高速信号保护应用中所需的低结电容(20pF)。

#### 应用

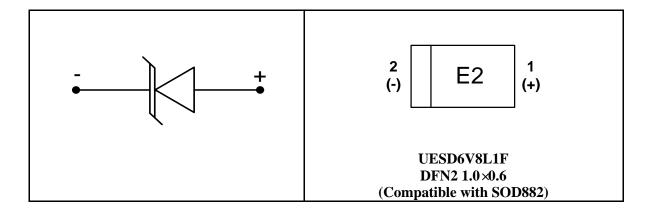
- 手机听筒和配件
- PDA
- 笔记本电脑、台式机和服务器
- 便携式设备
- 无线电话
- 数码相机
- 外围设备
- MP3播放器

#### 特性

- 数据线瞬态保护符合IEC 61000-4-2标准: ±15kV(空气间隙放电),±8kV(接触放电)
- 用于便携式电子设备的小型封装
- ESD保护应用中MLV的合适替代品
- 保护一路输入/输出或电源线
- 低钳位电压
- 反向工作电压: 5V
- 低漏电流
- 固态硅雪崩技术
- 小外形尺寸: 1.0mm×0.6mm

#### 引脚配置

#### 顶部视图



## **Ordering Information**

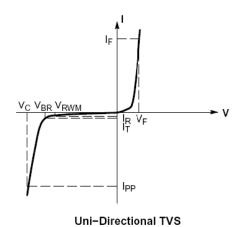
Part Number	Working Voltage	Packaging Type	Channel	Marking Code	Shipping Qty
UESD6V8L1F	5.0V	DFN2 1.0×0.6	1	E2	5000pcs/7 Inch Tape & Reel

## **Absolute Maximum Ratings**

Rating	Symbol	Value	Unit
Peak Pulse Power (t <sub>P</sub> =8/20μs)	$P_{PK}$	55	Watts
Maximum Peak Pulse Current (t <sub>P</sub> =8/20μs)	$I_{PP}$	10.8	Amps
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	$V_{PP}$	±15 ±8	kV
Lead Soldering Temperature	$T_{\rm L}$	260 (10 sec.)	$\mathcal C$
Operating Temperature	$T_{J}$	-55 to +125	$\mathcal C$
Storage Temperature	$T_{STG}$	-55 to +150	$\mathcal C$

## **Symbol Definition**

Parameter	Symbol
Maximum Reverse Peak Pulse Current	$ m I_{PP}$
Clamping Voltage @ I <sub>pp</sub>	$V_{\rm C}$
Working Peak Reverse Voltage	$ m V_{RWM}$
Maximum Reverse Leakage Current @ V <sub>RWM</sub>	$I_R$
Breakdown Voltage @ I <sub>T</sub>	$ m V_{BR}$
Test Current	$I_t$
Forward Current	$I_{\mathrm{F}}$
Forward Voltage @ I <sub>F</sub>	$ m V_F$
Peak Power Dissipation	$P_{PK}$
Max. Capacitance @ V <sub>R</sub> =0V, f=1MHz	C



PEAK VALUE I\_{RSM} @ 8  $\mu s$ 90 % OF PEAK PULSE CURRENT PULSE WIDTH (tp) IS DEFINED AS THAT POINT WHERE THE PEAK CURRENT DECAY = 8 µs 80 70 60 · HALF VALUE I<sub>RSM</sub>/2 @ 20 μs 50 40 30 20 10 0 L 20 40 t, TIME (μs)

# **UESD6V8L1F**

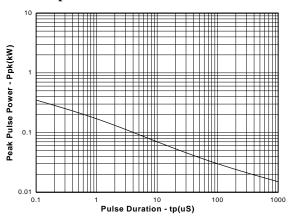
#### **Electrical Characteristics**

(T=25 ℃, Device for 5.0V Reverse Stand-off Voltage)

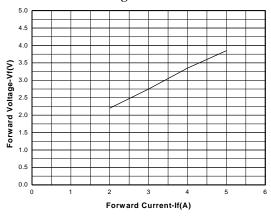
Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Reverse Stand-Off Voltage	$V_{\mathrm{RWM}}$				5	V
Reverse Breakdown Voltage	$V_{\text{BR}}$	I <sub>T</sub> =1mA	6	6.8	7.2	V
Reverse Leakage Current	$I_R$	$V_{RWM}=5V$ , $T=25$ °C			0.1	μΑ
		$I_{PP}=1A, t_{P}=8/20 \mu s$			7	
Clamping Voltage	$V_{C}$	$I_{PP}=2A, t_{P}=8/20 \mu s$			8	V
		$I_{PP}=5A, t_{P}=8/20 \mu s$			10.8	
Forward Voltage	$V_{\mathrm{F}}$	$I_F = 10 \text{mA}$		0.8		V
Junction Capacitance	$C_{J}$	$V_R=0V$ , $f=1MHz$		17	20	pF
Junction Capacitance	$C_{J}$	$V_R=2.5V$ , $f=1MHz$		8	10	pF

## **Typical Operating Characteristics**

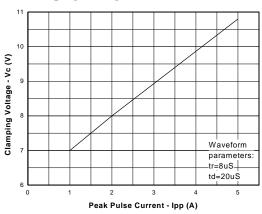
#### Non-Repetitive Peak Pulse Power vs. Pulse Time



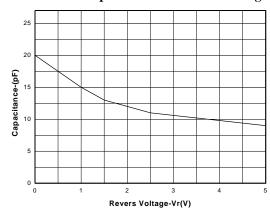
#### Forward Voltage vs. Forward Current



#### Clamping Voltage vs. Peak Pulse Current



#### Junction Capacitance vs. Reverse Voltage





## **UESD6V8L1F**

#### **Application Information**

#### **Device Connection Options**

UESD6V8L1F ESD protection diode is designed to protect one data, I/O, or power supply line. The device is unidirectional and may be used on lines where the signal polarity is above ground. The cathode dot should be placed towards the line that is to be protected.

#### Circuit Board Layout Recommendations for Suppression of ESD

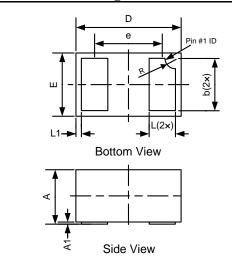
Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

- 1. Place the TVS near the input terminals or connectors to restrict transient coupling.
- 2. Minimize the path length between the TVS and the protected line.
- 3. Minimize all conductive loops including power and ground loops.
- 4. The ESD transient return path to ground should be kept as short as possible.
- 5. Never run critical signals near board edges.
- 6. Use ground planes whenever possible. For multilayer printed-circuit boards, use ground vias.
- 7. Keep parallel signal paths to a minimum.
- 8. Avoid running protection conductors in parallel with unprotected conductor.
- 9. Minimize all printed-circuit board conductive loops including power and ground loops.
- 10. Avoid using shared transient return paths to a common ground point.

## **Package Information**

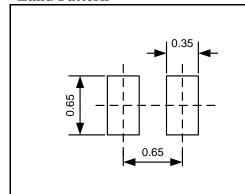
### **UESD6V8L1F DFN2 1.0×0.6**

**Outline Drawing** 



DIMENSIONS							
Symbol	MILLIMETERS			INCHES			
	Min	Тур	Max	Min	Тур	Max	
A	0.40	-	0.53	0.016	-	0.021	
A1	0.00	-	0.05	0.000	-	0.002	
b	0.45	0.50	0.55	0.018	0.020	0.022	
D	0.95	1.00	1.075	0.037	0.039	0.042	
Е	0.55	0.60	0.675	0.022	0.024	0.027	
e	(	0.65TY	P	0.026TYP			
L	0.20	0.25	0.30	0.008	0.010	0.012	
L1	0.00	0.05	0.10	0.000	0.002	0.004	
R	0.05	0.10	0.15	0.002	0.004	0.006	
Note: R is optional.							

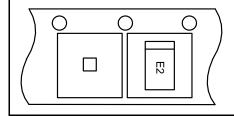
#### **Land Pattern**



#### NOTES:

- 1. Compound dimension: 1.00×0.60;
- 2. Unit: mm;
- 3. General tolerance ±0.05mm unless otherwise specified;
- 4. The layout is just for reference.

#### **Tape and Reel Orientation**





## **UESD6V8L1F**

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