Level Shifter for Multi Voltage Rail I/O Interconnection

Union Semiconductor, Inc.

Introduction

Level shifter circuits are the bridges that connect low core voltage components to high I/O interface voltage circuits. The UM320X and UM330X series level translator are designed to cost effectively address these voltage translation needs with high integration components. To achieve high performance and high integration density, the transistor dimensions are aggressively scaled down with an ultra deep submicron process. Low power dissipation is achieved by scaling down the supply voltage under 1.0V.

TheUM330X series are buffered type auto direction sensing voltage translator architectures, while UM320X series are switch type auto direction sensing voltage translator architectures. Neither type of architecture requires a DIR control signal to establish the direction of data flow. The buffered type architecture is designed to be exclusively connected and interfaced with a push-pull driver and is capable of driving light capacitive or high impedance loads. Switch type translators that are designed to interface with open drain drivers, such as the I^2C bus.

The need for voltage level translation

Voltage level translation is becoming increasingly significant in today's electronic systems. Digital switching level standards have continued to progress toward different voltage levels, resulting in system incompatibilities. For two devices to interface reliably, the output driver voltages must be compatible with receiver input thresholds. For this condition to be met in mixed voltage systems, a voltage translator circuit is often required. Similar incompatibilities can result from interfacing circuits with different ground references.

Fig 1.shows the reference circuit for the level-shifted Atmel® ATA6870 SPI. This reference circuit was implemented using the Atmel ATA6870-DK application kit. The kit consists of two application boards: the AVR® host controller and the Atmel ATA6870-DK battery management board. Since the AVR host controller and the battery management board are referenced to different ground potentials (GND_AVR and GND_BMS), the SPI and system clock lines must be level shifted between the two boards for communication to occur.

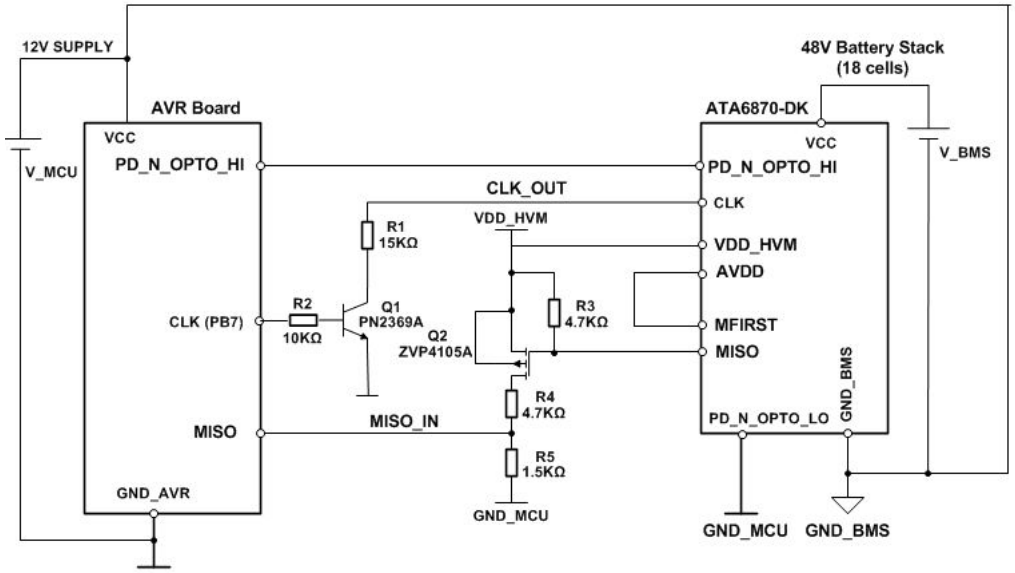

Figure 1.Atmel ATA6870-DK level shifted SPI implementation

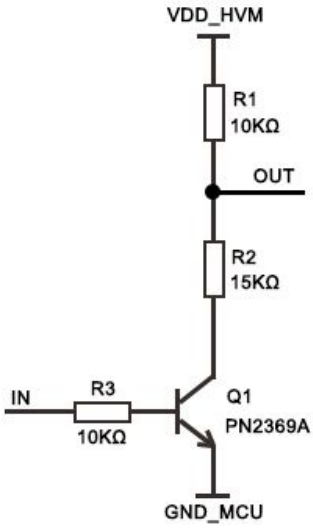

Figure 2.Input level shifter

Input level shifting from the microcontroller to the Atmel® ATA6870 is accomplished through the use of the circuit shown in Figure 2. All Atmel ATA6870 input SPI signals (SCK, MOSI, CS_N) and the system reference clock (used by the ADC) must use this circuit. The level shifter utilizes a high-speed switching NPN transistor and voltage divider to up-convert the low-level

microcontroller output voltage to the regulated, pulled-up Atmel ATA6870 voltage, VDDHVM (3.3V + VMCU).

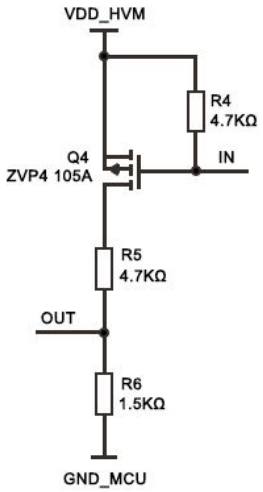

Figure 3.Output level shifter using discrete components.

Output level shifting from the Atmel ATA6870 to the microcontroller is accomplished by the circuit shown in Figure 3. All Atmel ATA6870 output SPI signals must use this circuit. The level shifter utilizes a switching PMOS transistor and a voltage divider to down-convert the Atmel ATA6870-DK output signal to the input voltage required by the microcontroller.

The UM330X translators are designed to replace the above discrete circuits to offer an integrated solution with reduced parts count.

UM320X translators are for replacing the discrete circuit shown in Fig 4 to interface with open drain drivers and used in applications, such as I^2C bus.

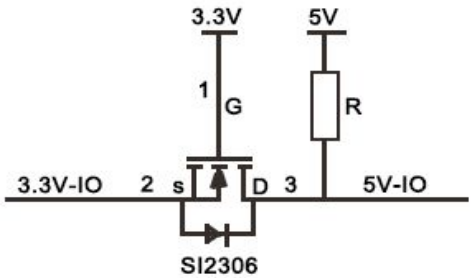

Figure 4. Switch type level shifter using discrete components

The UM330X and UM320X family of voltage translators

Union's push-pull buffered type UM330X translators are designed to exclusively be connected and interfaced with push-pull CMOS drivers. They are capable of driving a light capacitive or high impedance loads in applications such as SDIO or SPI bus.
Open-drain switch typeUM320X translators are designed to interface with open-drain drivers and used in applications such as I^2C bus.

Table 1 summarizes Union Semi's level shifter product offerings. Union offers 2, 4, 8 bit width devices supplied in CSP, QFN and TSSOP packages.

Product P/N	Brief Description	VCCA Range	VCCB Range	Max Data Rate (Mbps)	B Port ESD Rating (KV)	Package
UM3302H	2 Bit, Push Pull Buffer Type	1.2~3.6	1.65~5.5	100	±15	CSP2010-8
UM3304H	4 Bit, Push Pull Buffer Type	1.2~3.6	1.65~5.5			CSP2015-12
UM3304Q		1.2~3.6	1.65~5.5			QFN3030-14
UM3304QT		1.2~3.6	1.65~5.5			QFN2816-16
UM3308	8 Bit, Push Pull Buffer Type	1.2~3.6	1.65~5.5			CSP3025-20
UM3202H	2 Bit, Open Drain Switch Type	1.65~3.6	1.65~5.5	24 Mbps(Push Pull) 2 Mbps(Open Drain)	±15	CSP2010-8
UM3202Q		1.65~3.6	1.65~5.5			DFN1713-8
UM3202A		1.65~3.6	1.65~5.5			QFN1814-10
UM3204H	4 Bit, Open Drain Switch Type	1.65~3.6	1.65~5.5			CSP2015-12
UM3204Q		1.65~3.6	1.65~5.5			QFN3030-14
UM3204UE		1.65~3.6	1.65~5.5			TSSOP14

Figure 5 shows the basic architecture block diagram of a single channel of the UM330X device.

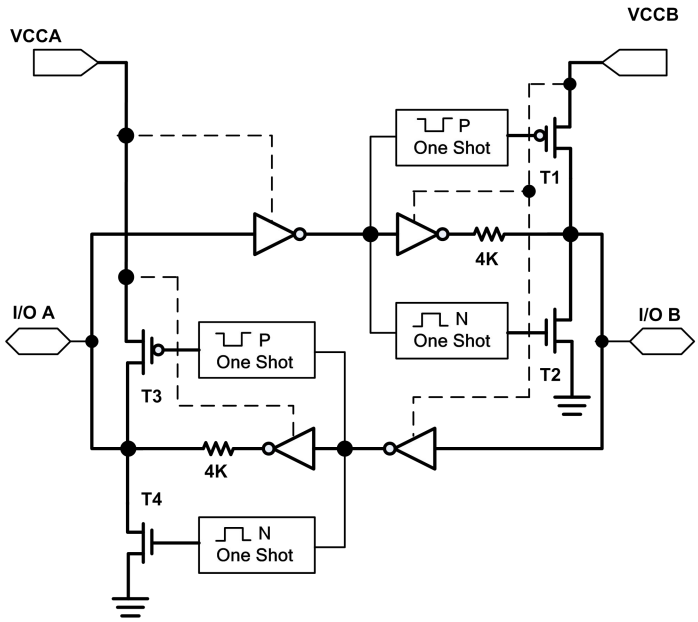

Figure 5. Block diagram for one of UM330X channel

In a DC state, the output drivers of the UM330X can maintain a high or low logic state. The drivers are designed to be weak so that they can be overdriven by an

external driver when data on the bus starts to flow in the opposite direction. The output of the one-shot detects rising or falling edges on the A or B port. During a rising edge, the one-shot turns on the PMOS transistors(T1,T3) for a short duration, this speeds up the low-to-high transition. Similarly, during a falling edge, a one shot turns on the NMOS transistors(T2,T4) for a short duration, this speeds up the high-to-low transition. One shot circuits improve signal integrity for optimum duplication of the original signal.

The basic block diagram architecture of a single channel of UM320X series is shown in Figure 6.

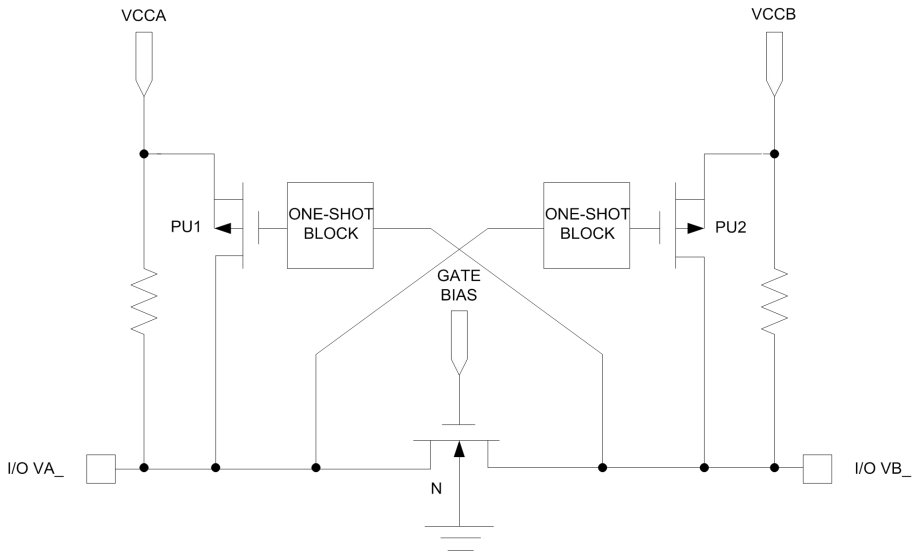

Figure 6. Block diagram of UM320X I/O Cell

The UM320X translators are FET-based architectures that use an N-channel pass-gate tansistor to open and close the connection between the A-port and B-port. When a driver connected to A or B port is low, the opposite port is, in turn, pulled low by the N pass-gate transistor. This pass-transistor type voltage translator is ideal for down-translation and over-voltage protection. Each A-port I/O has an internal pull-up resistor to VCCA, and each B-port I/O has an internal pull-up resistor to VCCB. During a rising edge, the one-shot turns on the PMOS transistors(PU1,PU2) for a short duration,which speeds up the low-to-high transition.

Integrated one shots in the Union UM330X and UM320X dramaticaly improve transition times over discrete component implementations. Fig 7 is waveform from translator circuit using discrete component.

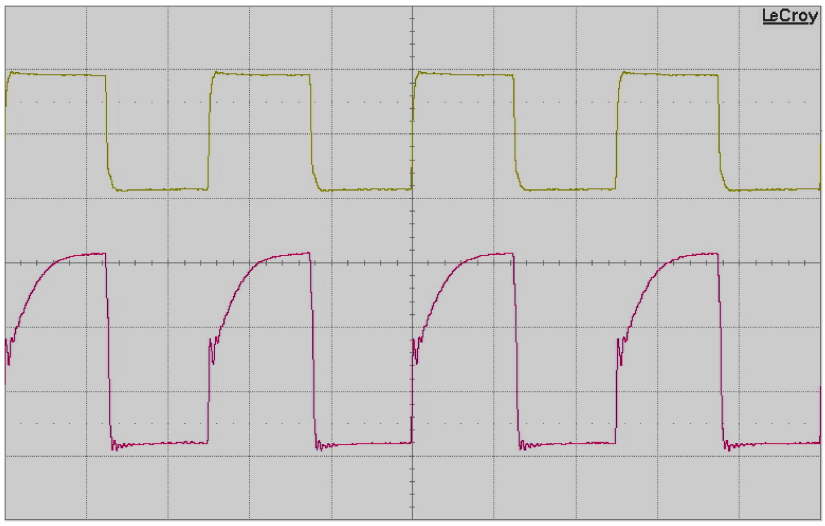

Figure 7. 1.8V to 3.3V conversion using discrete components, f=400KHz, 1us/div horizontal, 1V/div vertical

Fig 8's waveform exhibits higher integrity using integrated solution.

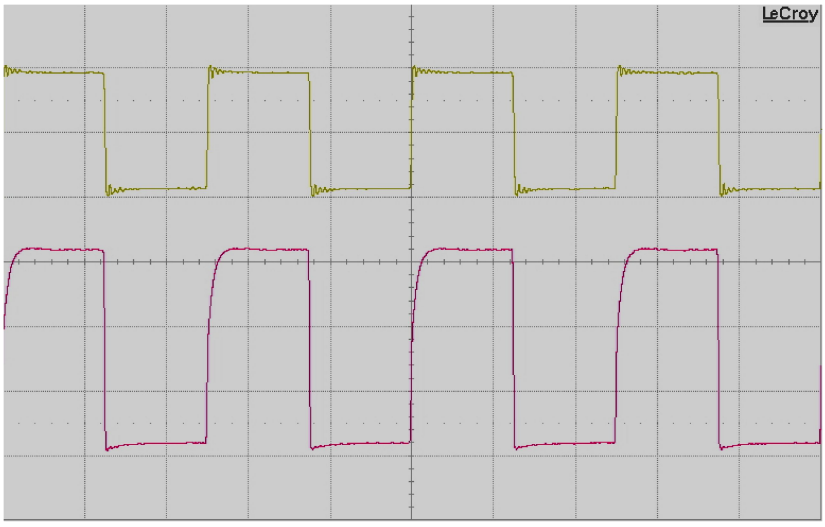

Figure 8. 1.8V to 3.3V conversion using UM3202 , f=400KHz, 1us/div horizontal, 1V/div vertical

The UM320X and UM330X both have an OE input that is used to disable the device by setting OE=low, which places all I/O's in the high impedance(Hi-Z)state.

When the output enable is high, the UM320X device consumes low power about 14uA while UM330X is 5uA. When the output enable is low, the UM320X and UM330X translator buffer will be disabled and the outputs are put into a high impedance stage for increased power saving. The OE input circuit is referenced to the V_{CCA} power supply and when the device is disabled, the pull-up resistors are disabled in UM320X, and the 4k Ω buffer and the one-shot for both the A-port and B-Port are also disabled in UM330X. If the application does not require output enable control, the OE pin should be tied to the V_{CCA} supply. The designer should never leave the OE pin floating.

Under partial power down (VCCA or VCCB = 0) conditions, the outputs are also disabled and put into a high-impedance state. This feature is referred to as VCC isolation, if VCCB=0V, the A-Port is disabled; likewise, if VCCA=0V, the B-Port will be disabled. This cut-off circuitry disables the outputs preventing damaging current backflow through the device when these devices are powered-down.

These translators were architected for driving high-impedance loads. The one-shot duration has been set to best optimize trade-offs of dynamic current consumption(ICC), load driving capability, and maximum bit-rate considerations. Careful PCB layout practice, with short trace lengths, should be followed to avoid excessive capacitive loading. To accomplish this, PCB signal trace-lengths should be kept short enough, such that the round trip delay of any reflection is less than the one-shot duration. This improves signal integrity by ensuring that any reflection sees a low impedance at the source driver. The one-shot circuits are designed to stay on for 10 to 30 ns.

There is a tradeoff between achieving a maximum data rate and driving heavy capacitive loads simultaneously. With heavy capacitive loads, the one-shot can time-out before the signal is driven fully to the positive rail. In this scenario, only the pull-up resistors will pull the line high by the RC time-constant of resistive and capacitive loadings. It is best to avoid this condition by driving capacitive loads less than 70pF when maximum data rate are desired.

If the application requires an external pull-up or pull-down resistor, special consideration must be given to the resistor value. It is important to choose a large enough resistor to ensure adequate V_{OH} and V_{OL} levels at the output port of the translator. With regard to capacitive loads, the translators are designed to drive up to 70 pF without issue.

PCB design guidelines for dual power supply voltage level shifter

The design of the PCB is an important factor in maximizing the performance of a dual power supply voltage translator. Good PCB design should include:

- Effective power supply decoupling is provided by placing ceramic capacitors next to the IC with minimum length connection traces

- Short PCB traces and ground planes reduce RF susceptibility and radiated emissions

Effective implementation of decoupling capacitors is critical to the noise immunity of the level translator. Short current transients, caused by high speed switching in CMOS circuits, cause problems such as glitches on the output voltage signals.

Figure 9 provides an example of the recommended locations of the VL and VCC decoupling capacitors. Ceramic capacitors with a magnitude of 0.01 μ F to 0.1 μ F are a good choice because they are inexpensive, small and have excellent high frequency attenuation specifications. Ground and power planes are one option commonly used to provide short, low impedance trace connections.

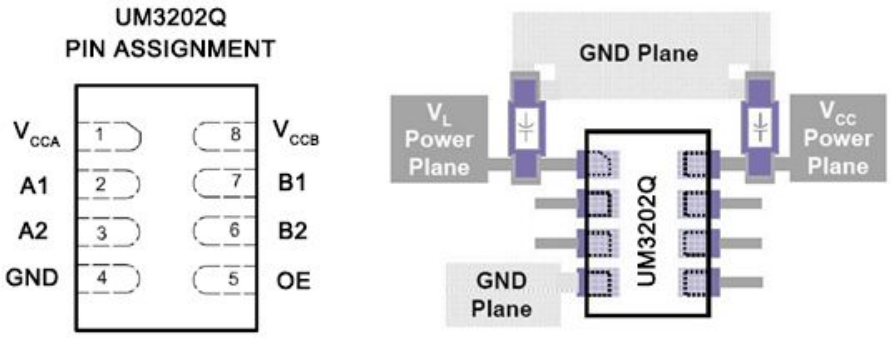

Figure 9. Effective power supply decoupling is provided by locating the capacitors as close as possible to the VL and VCC power pins while providing a low impedance ground connection

RF susceptibility and radiated emissions can be reduced by minimizing the loop area formed by high speed data and ground lines. This can be done by shortening the translator's I/O-to-connector trace lengths and utilizing a ground plane in the PCB design.

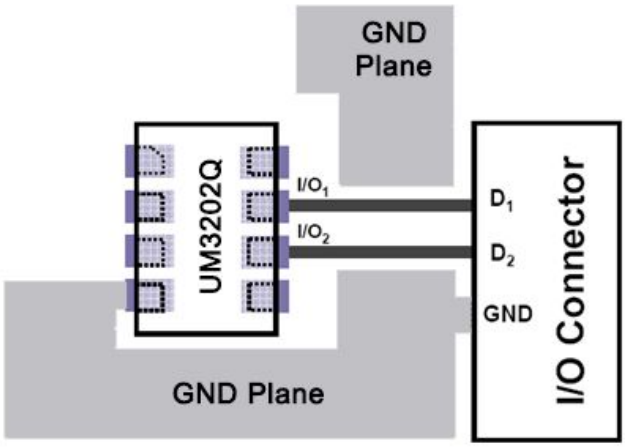

Figure 10. Short PCB traces and ground planes decrease RF susceptibility and emissions.

Conclusion

Core logic supply voltages are being scaled down aggressively to achieve low power dissipation, while legacy I/O interface components continue to require higher voltages. Maintaining voltage compatibility and signal integrity requires new low cost solutions. Union Semi's UM330X and UM320X series voltage translator offers system designers a compact and high signal integrity solution to remedy mixed voltage system incompatibilities. These translators eliminate the need for an extra direction control pin. This can simplify the software and hardware design as well as reduce parts count.