RELIABILITY REPORT

FOR

UM3699

PLASTIC ENCAPSULATED DEVICES

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UNION INTEGRATED PRODUCTS

Written by

Sindy Bi
Quality Assurance
Engineer

Reviewed by

Tina Liu
Quality Assurance
Executive Director

Conclusion

The UM3699 successfully meets the quality and reliability standards required of all Union products. In addition, Union's continuous reliability monitoring program ensures that all outgoing products will continue to meet Union's quality and reliability standards.

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I. Device Description

A. General

The UM3699 dual independent ultra low R_{ON} DPDT analog switch operates from a single +1.65V to +5.5V supply. It features a 0.6Ω (max) R_{ON} for its NO and NC switch at a +3.0V supply.

The UM3699 features break-before-make switching action (15ns) with t_{ON}=50ns and t_{OFF}=30ns at +4.5V. The device has a 3.8KΩ internal shut resistors that automatically discharge the capacitance at the normally open (NO) and normally closed (NC) terminals when they are not connected. This reduces click-and-pop noises that occur when switching audio signals between precharged points.

B. Absolute Maximum Ratings

Item	Rating
V_{CC}, $V_{IN_}$	-0.5V to +5.5V
NO_, NC_, COM_ (Note 1)	-0.5V to V_{CC}
Continuous Current from COM_ to NO_/NC_	±300mA
Peak Current from COM_ to NO_/NC_ (10% duty cycle)	±500mA
Storage Temperature	-65°C to +150°C
Lead Temp. (Soldering, 30S)	+260°C

Note 1: Signals on NO_, NC_, and COM_ exceeding V_{CC} or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

II. Manufacturing Information

A. Description/Function: Ultra-Low R_{ON}, Dual DPDT Analog Switch

B. Process: Standard 0.35 micron silicon gate CMOS

C. Number of Device Transistors: 5176

D. Fabrication Location: Suzhou, Jang Su province, China

E. Assembly Location: KH (Diodes Shanghai)

F. Date of Initial Production: Dec, 2007

III. Packaging Information

A. Package Type: QFN16

B. Lead Frame: Cu (C7025HH)

C. Lead Finish: Ni/Pd/Au

D. Die Attach: Epoxy(QM1519)

E. Bondwire: Gold (1.0 mil diameter)

F. Mold Material: EME-G770H-HCD

G. Assembly Diagram: Attachment: AD-KH-UM3699

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: Level 1

IV. Die Information

A. Dimensions: 60 x 60 mils

B. Passivation: Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Si (Si=1%)

D. Backside Metallization: None

E. Minimum Metal Width: 0.5 microns

F. Minimum Metal Spacing: 0.5 microns

G. Bondpad Dimensions: 3.5 mil. Sq.

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% for all Visual Defects.

B. Observed Outgoing Defect Rate: < 50 ppm

C. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 125℃ biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{2 \times 77 \times 168 \times 2502}$$ (Chi square value for MTTF upper limit)

2502 — At: thermal acceleration factor assuming a 0.8eV activation energy

$$At = \exp\left(\frac{E_A}{k}\right)\left(\frac{1}{T2} - \frac{1}{T1}\right)$$

E_A=Average thermal activation energy for expected failure mechanisms=0.8eV
k= Boltzmann's constant= 8.62×10^{-5} eV/K
T1= Life test operating temperature=125℃
T2= System use operating temperature=25℃

$\lambda = 28.27 \times 10^{-9}$

F.I.T.=28.27 (60% confidence level @ 25°C)

This low failure rate represents data collected from Union's reliability monitor program. In addition to routine production Burn-In, Union pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Union performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Attachment 4#: BI-KH-UM3699) shows the static Burn-In circuit.

B. Moisture Resistance Tests

Union pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C /85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The UW002 die type has been found to have all pins able to withstand a transient pulse of ± 2000V, per Mil- Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±200mA and/or 9V.

Attachment #1

TABLE Ⅰ Reliability Evaluation Test Results

UM3699

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 125°C Biased Time = 168 hrs.	DC Parameters & functionality	77	0
Moisture Testing (Note 2)				
Pressure Pot	T = 121°C P = 15 PSIG RH= 100% Time = 96hrs.	DC Parameters & functionality	77	0
85/85 (Note 3)	T = 85°C RH = 85% Vr =100V Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles JESD22 A-104	DC Parameters	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.
Note 2: Generic Package/Process data
Note 3: Board Level

Attachment #2

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

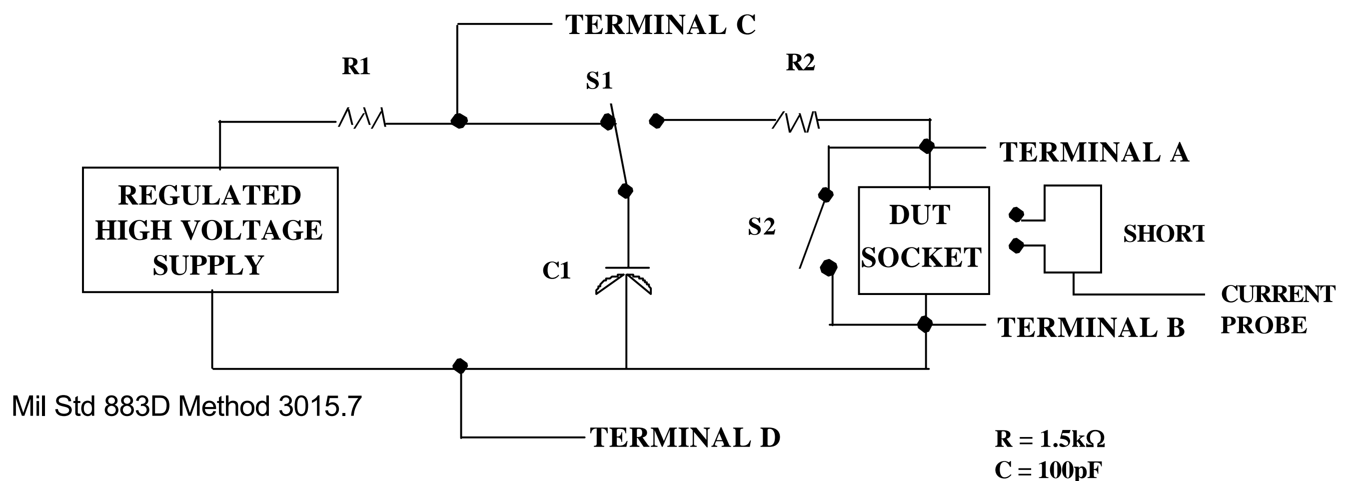
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combination to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

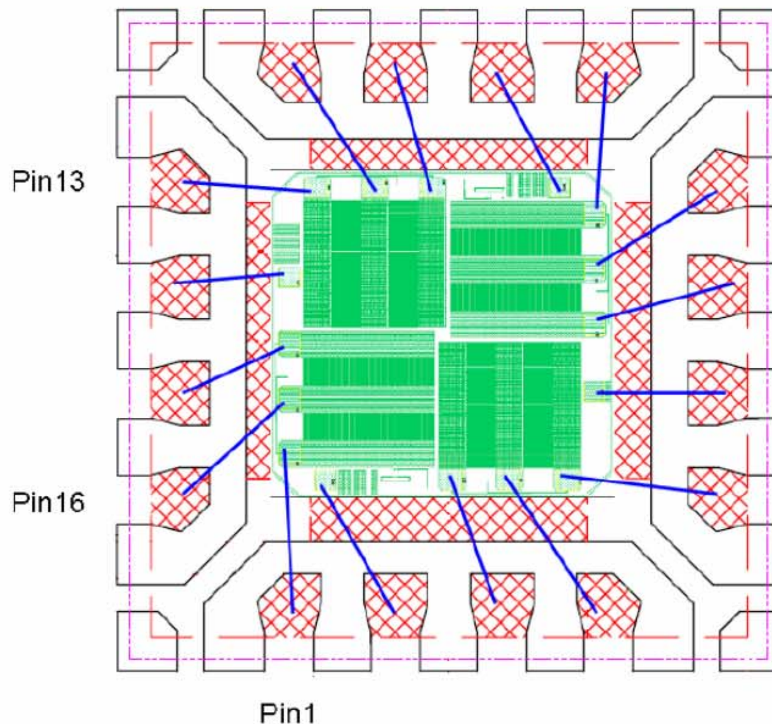
c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D Method 3015.7

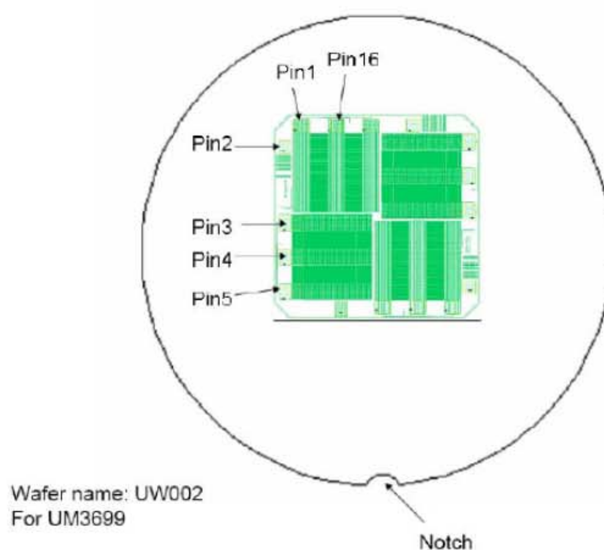
Attachment #3

1.2 打线图 Bonding diagram



Note: 芯片的 Pin 脚在 wafer 上的对应位置。

从晶圆正面(即有电路的一面)看, 放大某个芯片



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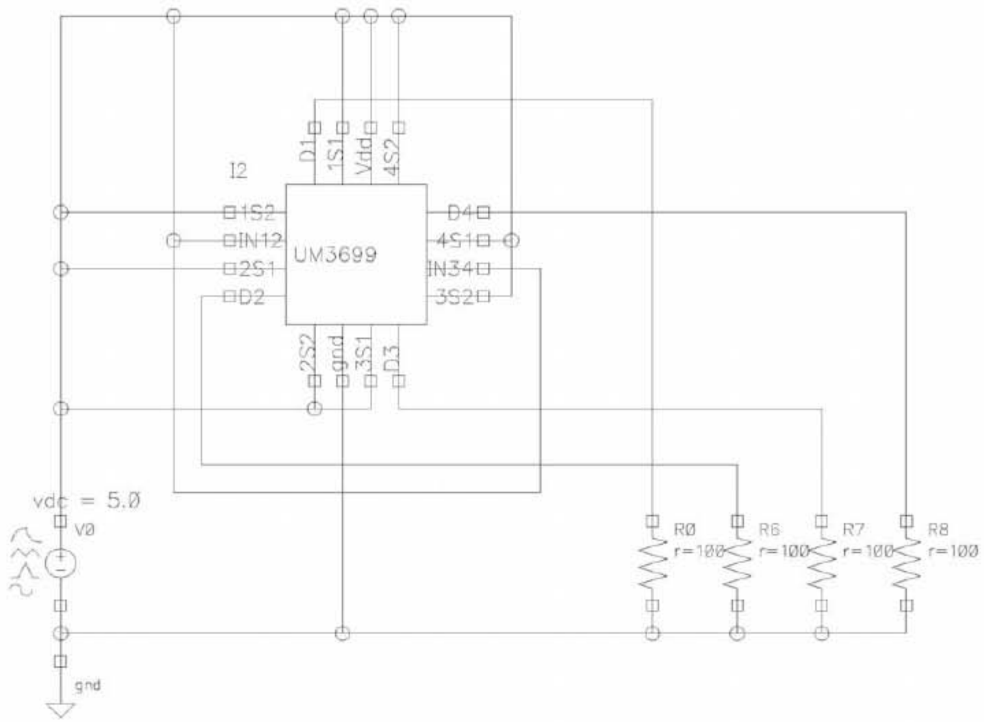
Attachment #4



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