

Quad Channel Low Capacitance ESD Protection Array

UM5304EEAF SC70-6/SC88/SOT363

UM5304EEBF SC89-6/SOT563/SOT666

UM5304EECF TSOP-6/SOT23-6

General Description

UM5304EEXF are surge rated diode arrays designed to protect high speed data interfaces. This series has been specifically designed to protect sensitive components which are connected to data and transmission lines from over-voltage caused by ESD (electrostatic discharge).

The unique design incorporates surge rated, low capacitance steering diodes in a single package. During transient conditions, the steering diodes direct the transient to either the positive side of the power supply line or to ground.

The low capacitance array configuration allows the user to protect four high-speed data or transmission lines. The low inductance construction minimizes voltage overshoot during high current surges. This device is optimized for ESD protection of portable electronics. They may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 ($\pm 15\text{kV}$ air, $\pm 8\text{kV}$ contact discharge).

Applications

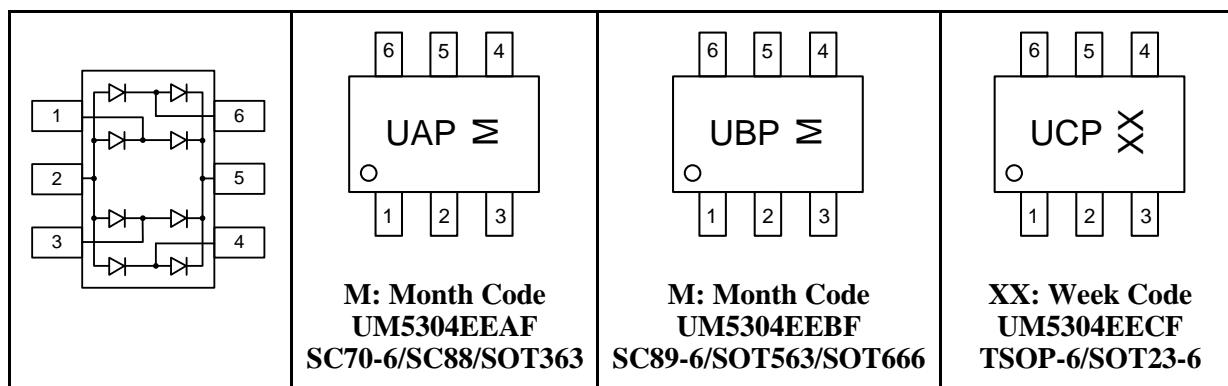
- USB 2.0
- USB OTG
- Monitors and Flat Panel Displays
- Digital Visual Interface (DVI)
- High-Definition Multimedia Interface (HDMI)
- SIM Ports
- IEEE 1394 Firewire Ports

Features

- Transient Protection for High-Speed Data Lines to IEC 61000-4-2 (ESD) $\pm 15\text{kV}$ (Air), $\pm 8\text{kV}$ (Contact)
- Array of Surge Rated Diodes
- Protects up to Four I/O Lines & Power Line
- Low Capacitance ($<2\text{pF}$) for High-Speed Interfaces
- No Insertion Loss to 2.0GHz
- Low Leakage Current and Clamping Voltage
- Low Operating Voltage: 5.0V

Pin Configurations

Top View



Ordering Information

Part Number	Working Voltage	Packaging Type	Channel	Marking Code	Shipping Qty
UM5304EEAF	5.0V	SC70-6/SC88/SOT363	4	UAP	3000pcs/7 Inch Tape & Reel
UM5304EEBF		SC89-6/SOT563/SOT666		UBP	
UM5304EECF		TSOP-6/SOT23-6		UCP	

Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Peak Pulse Power ($t_p=8/20\mu s$)	P_{pk}	150	Watts
Peak Pulse Current ($t_p=8/20\mu s$)	I_{pp}	6	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	± 15 ± 8	kV
Operating Temperature	T_J	-55 to +125	$^{\circ}C$
Storage Temperature	T_{STG}	-55 to +150	$^{\circ}C$

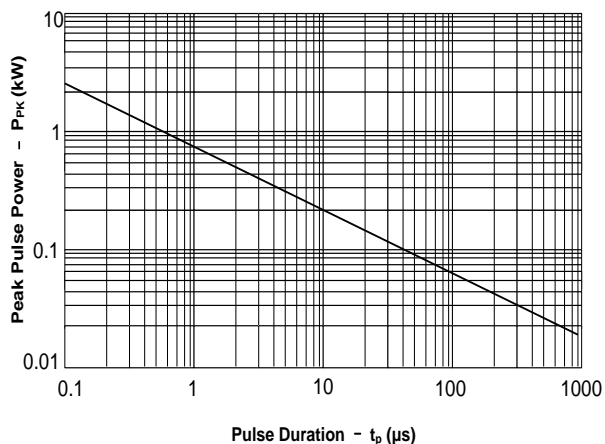
Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Reverse Stand-Off Voltage	V_{RWM}				5.0	V
Reverse Breakdown Voltage	V_{BR}	$I_T=1mA$, Pin 5 to 2	6.0			V
Reverse Leakage Current	I_R	$V_{RWM}=5V$, $T=25^{\circ}C$ Pin 5 to 2			2	μA
Clamping Voltage	V_C	$I_{pp}=1A$, $8/20\mu s$ Any Pin to Pin 2			15	V
Clamping Voltage	V_C	$I_{pp}=6A$, $8/20\mu s$ Any Pin to Pin 2			25	V
Junction Capacitance	C_j	$V_R=0V$, $f=1MHz$ Any I/O Pin to Pin 2 (Note 1)			2	pF
		$V_R=0V$, $f=1MHz$ Between I/O Pins (Note 1)			1	pF

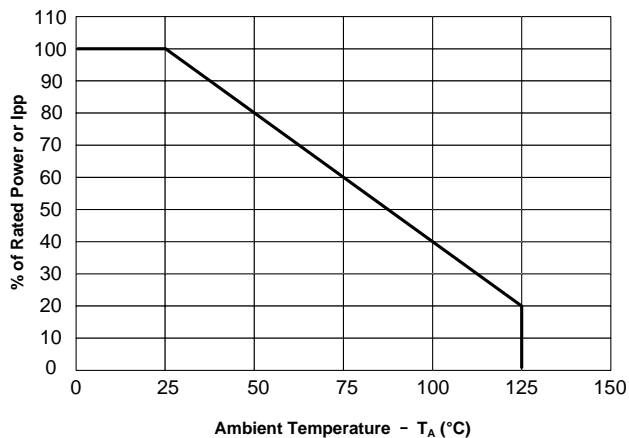
Note 1: I/O pins are pin 1, 3, 4 and 6

Typical Operating Characteristics

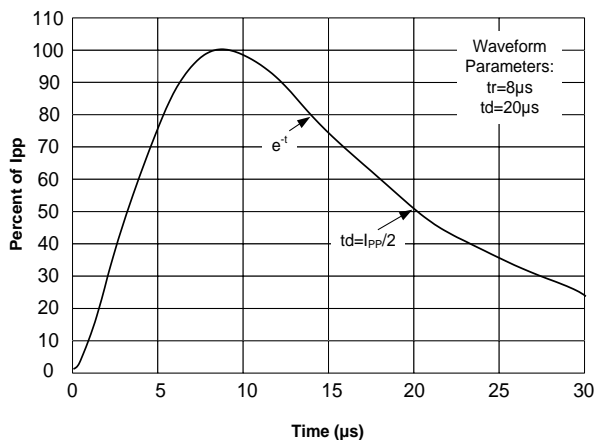
Non-Repetitive Peak Pulse Power vs. Pulse Time



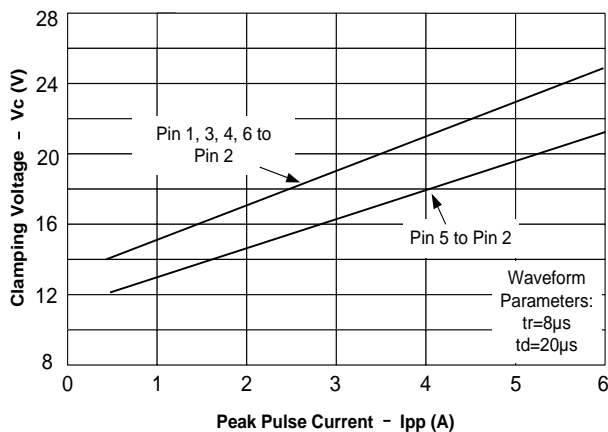
Power Derating Curve



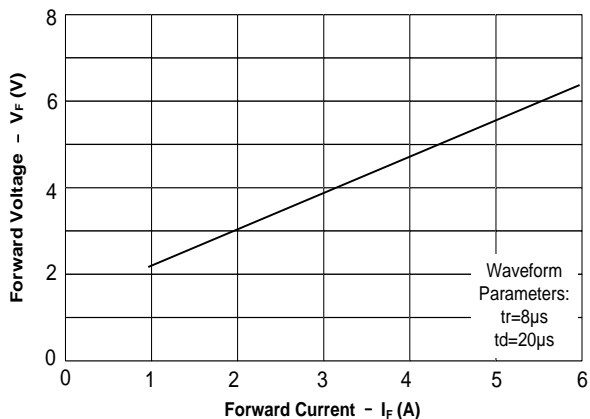
Pulse Waveform



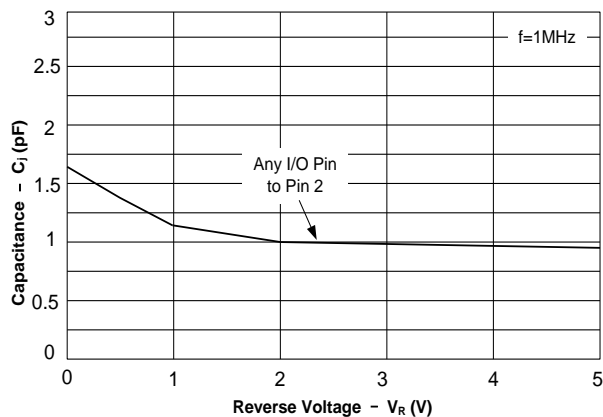
Clamping Voltage vs. Peak Pulse Current



Forward Voltage vs. Forward Current



Junction Capacitance vs. Reverse Voltage

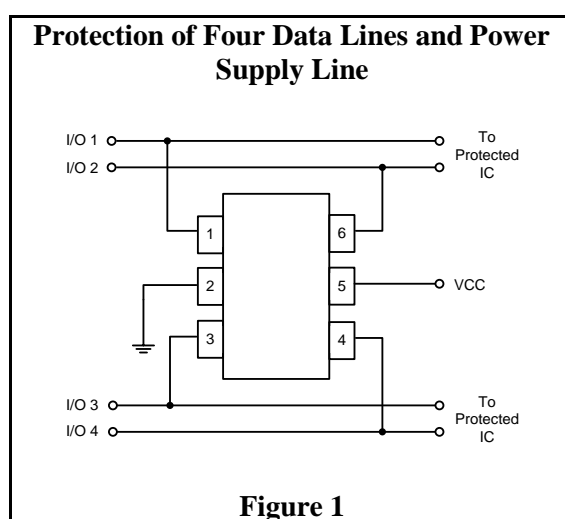


Applications Information

Device Connection Options for Protection of Four High-Speed Data Lines

This device is designed to protect data lines by clamping them to a fixed reference. When the voltage on the protected line exceeds the reference voltage the steering diodes are forward biased, conducting the transient current away from the sensitive circuitry. Data lines are connected at pins 1, 3, 4 and 6. Pin 2 should be connected directly to a ground plane. The path length is kept as short as possible to minimize parasitic inductance. The positive reference is connected at pin 5. The options for connecting the positive reference are as follows:

To protect data lines and the power line, connect pin 5 directly to the positive supply rail (VCC). In this configuration the data lines are referenced to the supply voltage. See Figure 1.



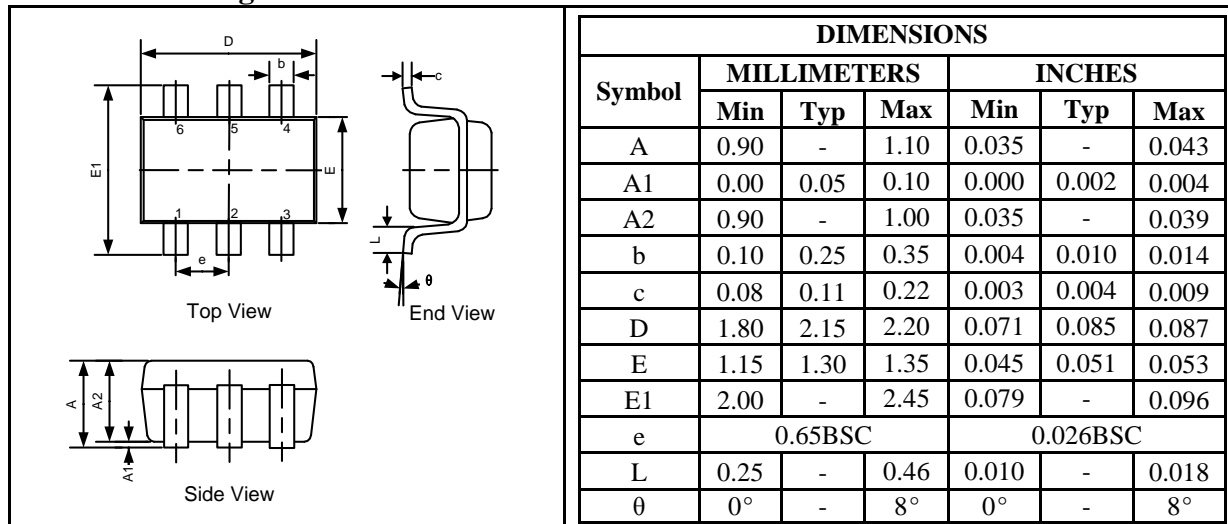
Matte Tin Lead Finish

Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. In addition, unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation of the solder joint.

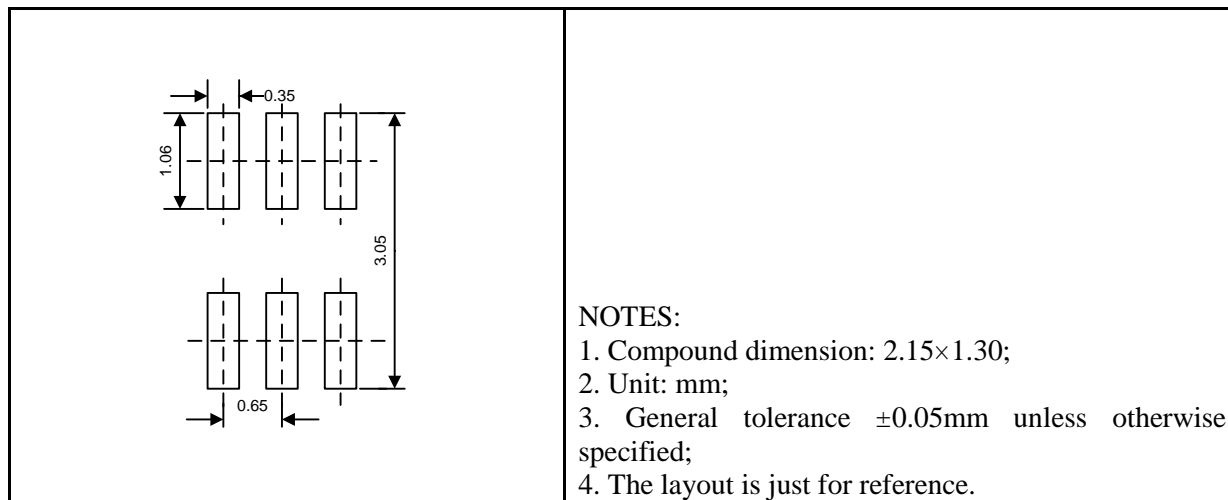
Package Information

UM5304EEAF SC70-6/SC88/SOT363

Outline Drawing



Land Pattern

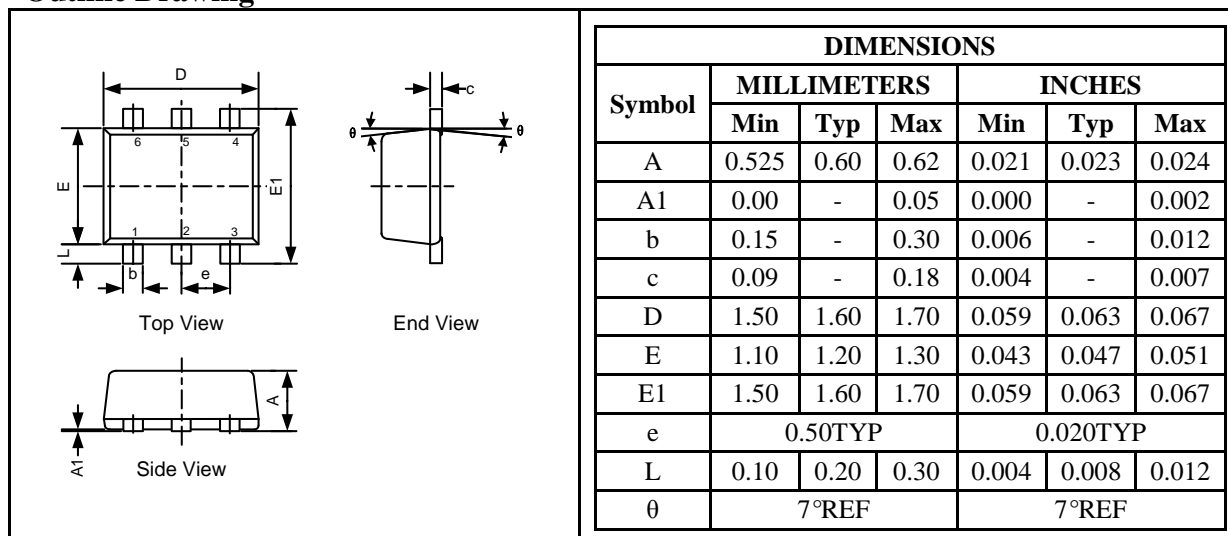


Tape and Reel Orientation

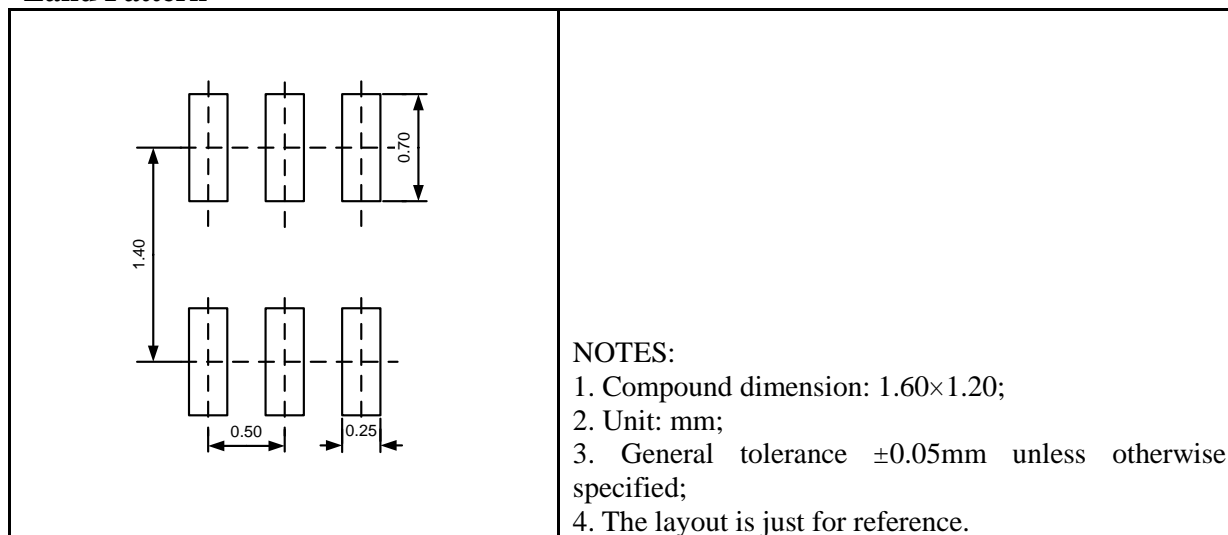


UM5304EEBF SC89-6/SOT563/SOT666

Outline Drawing



Land Pattern

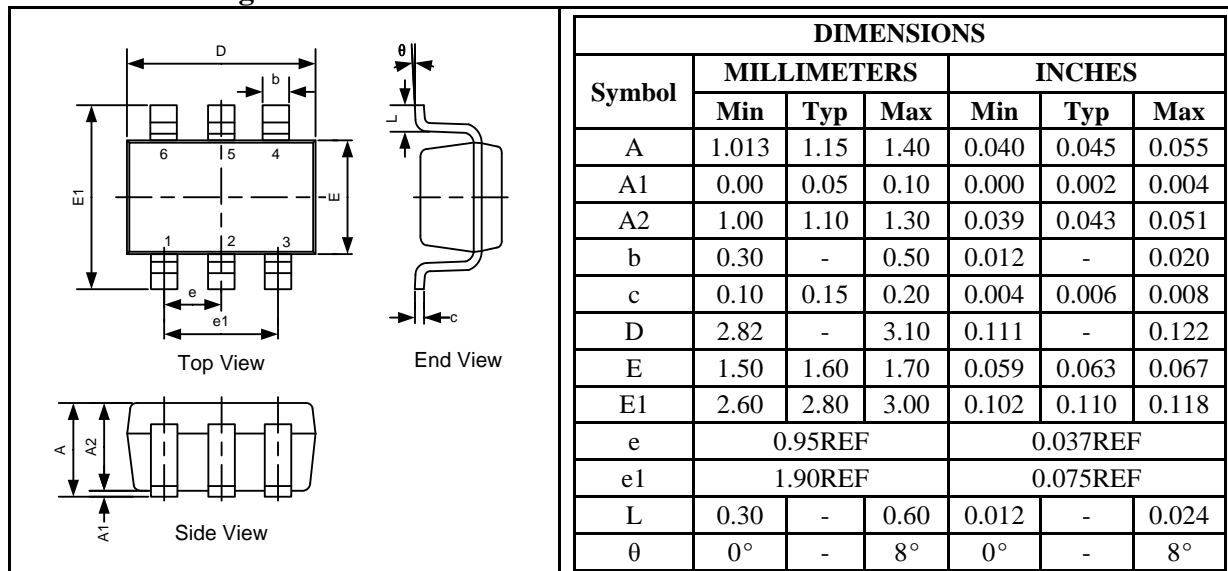


Tape and Reel Orientation

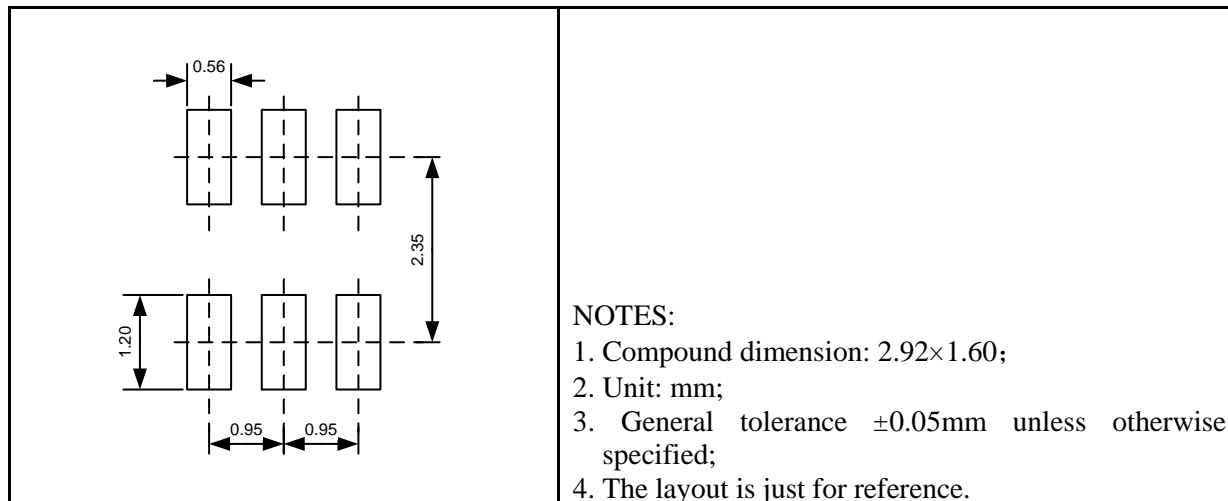


UM5304EECF TSOP-6/SOT23-6

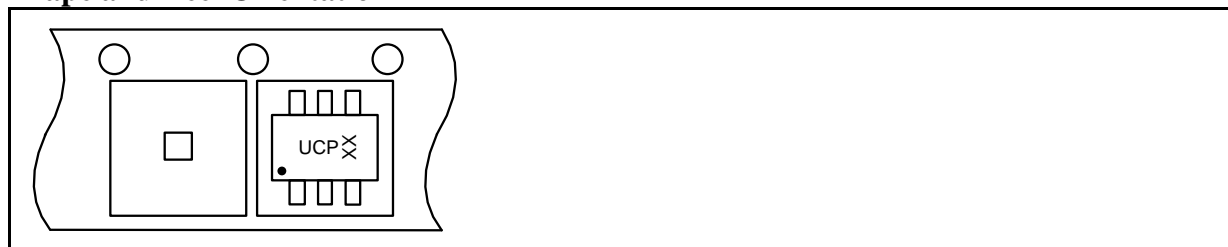
Outline Drawing



Land Pattern



Tape and Reel Orientation



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