

0.5Ω Ultra Low On-Resistance Dual SPDT Analog Switch

UM5223 QFN10 1.8×1.4

General Description

The UM5223 is a low on-resistance (R_{ON}), dual single-pole/double-throw (SPDT) analog switch operates from a single +1.65V to +4.5V supply. The device's targeted applications include battery powered equipment that benefit from its low on-resistance.

The UM5223 features two 0.5Ω $R_{ON(max)}$ SPDT switches with 0.15Ω flatness and 0.05Ω matching between channels. The switch offers break-before-make switching (1ns) with $t_{ON}<60ns$ and $t_{OFF}<40ns$ at +2.7V.

The switch is available in Pb-free QFN10 package.

Applications

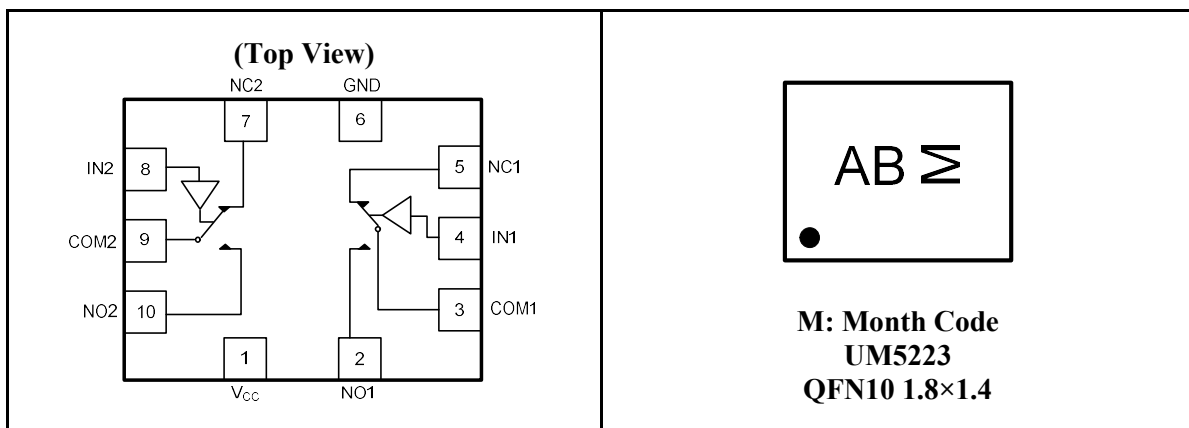
- Cell Phone Audio Block
- Speaker and Earphone Switching
- Portable Instrumentation
- Battery-Operated Equipment
- Modems
- Medical Equipment
- Computer Peripherals
- Ring-Tone Chip/Amplifier Switching

Features

- Ultra-Low $R_{ON}<0.5\Omega$ at $V_{CC}=3.0\pm 0.3V$
- R_{ON} Flatness of 0.15Ω
- Single-Supply Operation from +1.65V to +4.5V
- Control logic compatible with 1.8V logic
- Full 0-V_{CC} Signal Handling Capability
- Power Off Protection:
When $V_{CC}=0V$, Input Signal can Tolerate up to 4.5V
- High Off-Isolation: -78dB (100kHz)
- Low Crosstalk: -92dB (100kHz)
- Low Distortion: 0.12%
- High Continuous Current Capability:
±300mA through Each Switch
- Lead (Pb)-Free QFN10 Package

Pin Configurations

Top View



Pin Description

Pin	Name	Function
1	V _{CC}	Positive Supply Voltage
2	NO1	Analog Switch 1-Normally Open Terminal
3	COM1	Analog Switch 1-Common Terminal
4	IN1	Analog Switch 1-Digital Control Input
5	NC1	Analog Switch 1-Normally Closed Terminal
6	GND	Ground Connection
7	NC2	Analog Switch 2-Normally Closed Terminal
8	IN2	Analog Switch 2-Digital Control Input
9	COM2	Analog Switch 2-Common Terminal
10	NO2	Analog Switch 2-Normally Open Terminal

Ordering Information

Part Number	Packaging Type	Marking Code	Shipping Qty
UM5223	QFN10 1.8×1.4	AB	3000pcs/7 Inch Tape & Reel

Function Table

IN __	NO __	NC __
0	OFF	ON
1	ON	OFF

Absolute Maximum Ratings

Symbol	Parameter	Limit	Unit
V ₊	Supply Voltage	-0.3 to +4.6	V
V _S	DC Switch Voltage (Note 1)	-0.3 to (V ₊ +0.3)	
IN __	DC IN Voltage	-0.3 to +4.6	
I _o	Continuous Current (COM __ , NO __ , NC __)	±300	mA
I _p	Peak Current (Pulsed at 1ms, 10% Duty Cycle)	±500	
T _O	Operating Temperature Range	-40 to +85	°C
T _J	Junction Temperature	+150	
T _{STG}	Storage Temperature Range	-65 to +150	
T _L	Junction Lead Temperature (Soldering, 10 Seconds)	+300	
ESD	ESD Method 3015.7	>2000	V

Note 1: Signals on COM_{_}, NO_{_}, or NC_{_} exceeding V₊ or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

DC Electrical Characteristics

Symbol	Parameter	Test Conditions	V _{CC} (V)	Temp	Limits (-40°C to 85°C)			Unit
					Min	Typ	Max	
I _{IN}	Input Leakage Current	V _{IN} =3.6V or GND	3.6	Room Full	-0.1 -1.0		0.1 1.0	μA
I _{OFF}	Power Off Leakage Current	V _{IN} =3.6V or GND	0	Room Full	-0.5 -2.0		0.5 2.0	μA
I _{COM(ON)}	COM ON Leakage Current	V _{IN} =V _{IL} or V _{IH} V _{NO} 0.3V or 3.3V with V _{NC} Floating or V _{NC} 0.3V or 3.3V with V _{NO} Floating V _{COM} =0.3V or 3.3V	3.6	Room Full	-0.01 -0.1		0.01 0.1	μA
I _{NO/NC(OFF)}	OFF State Leakage Current	V _{IN} =V _{IL} or V _{IH} V _{NO} or V _{NC} =0.3V V _{COM} =3.3V	3.6	Room Full	-0.3		0.3	μA
I _{CC}	Quiescent Supply Current	Select V _{IS} =V _{CC} or GND	1.65 to 3.6	Room Full	-1.0 -2.0		1.0 2.0	μA
V _{IH}	Input High Voltage		3.0	Full	1.4			V
			3.6		1.7			
V _{IL}	Input Low Voltage		3.0	Full			0.7	V
			3.6				0.8	
R _{ON}	On-Resistance (Note 2)	V _{IN} =V _{IL} or V _{IH} V _{IS} =V _{CC} to GND I _{COM} =100mA	3.0	Room Full		0.5 0.6		Ω
			3.6	Room Full		0.5 0.6		
ΔR _{ON}	On Resistance Match Between Channels (Note 2,3,4)	V _{IS} =1.5V I _{COM} =100mA; V _{IS} =1.8V I _{COM} =100mA	3.0	Room Full			0.05 0.05	Ω
			3.6	Room Full			0.05 0.05	
R _{FLAT}	On Resistance Flatness (Note 2,3,5)	V _{IS} =V _{CC} to GND I _{COM} =100mA	3.0	Room Full			0.15 0.15	Ω
			3.6	Room Full			0.15 0.15	

Note 2: Guaranteed by design. Resistance measurements do not include test circuit or package resistance.

Note 3: Parameter is characterized but not tested in production.

Note 4: ΔR_{ON}=R_{ON(B0)}-R_{ON(B1)} measured at identical V_{CC}, temperature and voltage levels.

Note 5: Flatness is defined as the difference between the maximum and minimum value of On Resistance over the specified range of conditions.

AC Electrical Characteristics

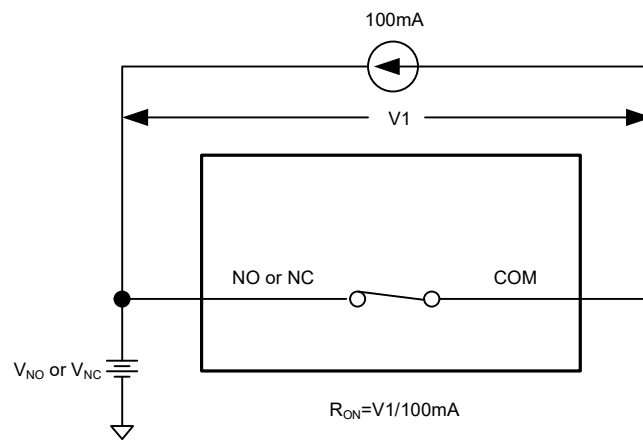
Symbol	Parameter	Test Conditions	V _{CC} (V)	Temp	Limits (-40°C to 85°C)			Unit
					Min	Typ	Max	
t _{ON}	Turn On Time	V _{IS} =1.5V R _L =50Ω, C _L =35pF	2.3 to 3.6	Room Full		50 60		ns
t _{OFF}	Turn Off Time	V _{IS} =1.5V R _L =50Ω, C _L =35pF	2.3 to 3.6	Room Full		30 40		ns
t _{BBM}	Break Before Make Time (Note 6)	V _{IS} =3.0V R _L =50Ω, C _L =35pF	3.0	Room Full	2	15		ns
Q _{INJ}	Charge Injection (Note 6)	C _L =1.0nF, V _{GEN} =0V, R _{GEN} =0Ω	1.65 to 3.6	Room		38		pC
V _{ISO}	Off Isolation (Note 7)	C _L =5.0pF, f=100kHz	1.65 to 3.6	Room		-78		dB
V _{CT}	Crosstalk	R _L =50Ω, C _L =5.0pF, f=100kHz	1.65 to 3.6	Room		-92		dB
BW	-3dB Bandwidth		1.65 to 3.6	Room		75		MHz
THD	Total Harmonic Distortion (Note 6)	f _{IS} =20Hz to 20kHz, R _L =R _{GEN} =600Ω C _L =50pF, V _{IS} =2.0V RMS	3.0	Room		0.12		%
Capacitance								
C _{IN}	IN Pin Input Capacitance (Note 8)	V _{CC} =3.6V				4.5		pF
C _{NO/NC}	NO/NC Port Off Capacitance (Note 8)	V _{CC} =3.6V				20		pF
C _{COM}	COM Port Capacitance when Switch is Enabled (Note 8)	V _{CC} =3.6V				55		pF

Note 6: Guaranteed by design.

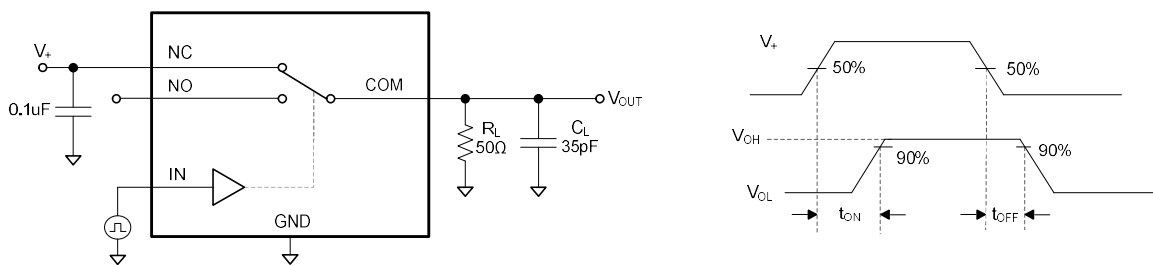
Note 7: Off Isolation=20 log₁₀ [V_{COM}/V_{NO/NC}].

Note 8: T_A=+25°C, f=1MHz, Capacitance is characterized but not tested in production.

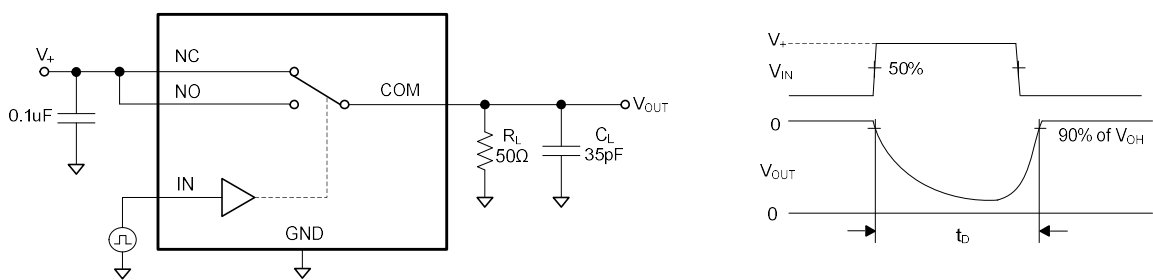
Test Circuits



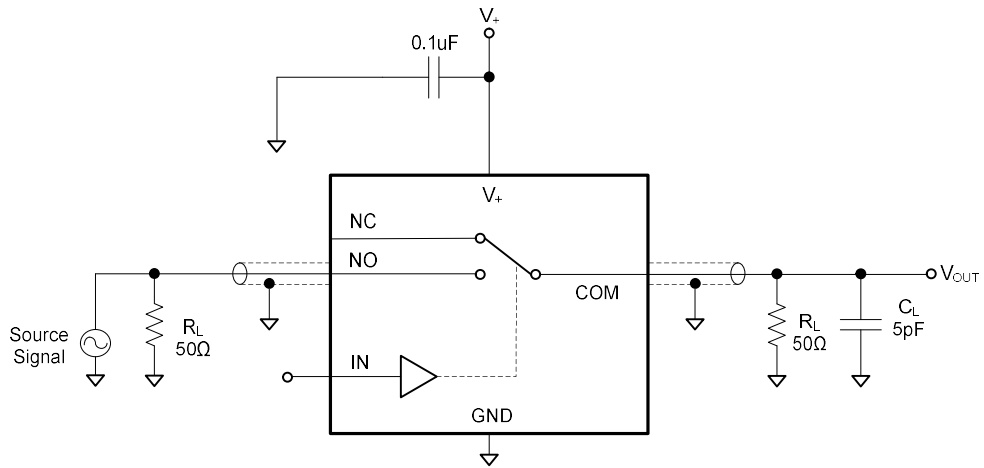
Test Circuit 1. On Resistance



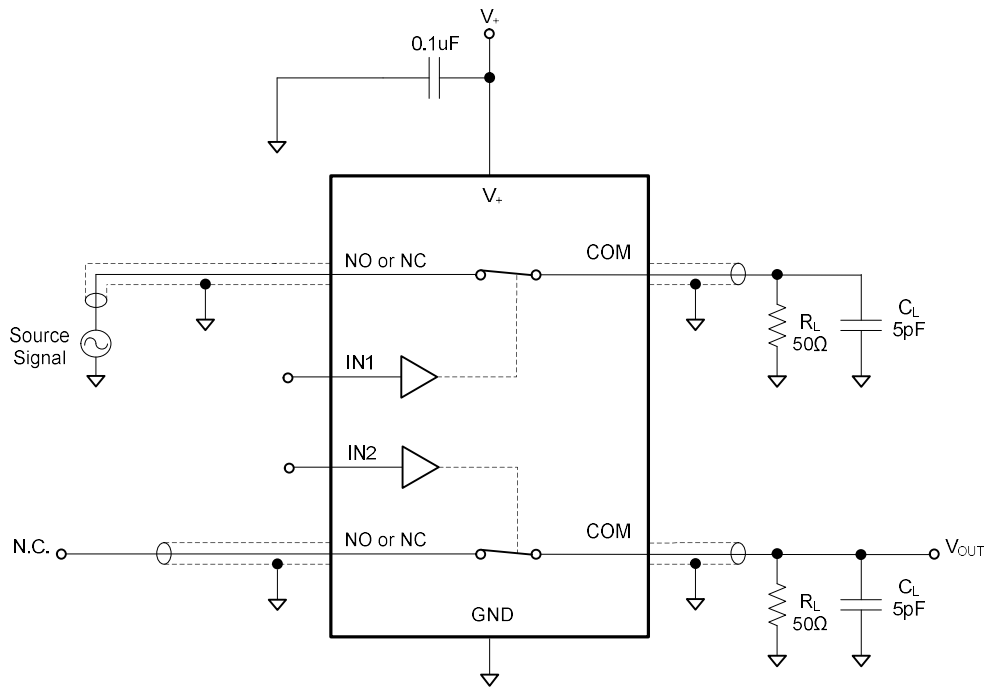
Test Circuit 2. Switching Times (t_{ON}, t_{OFF})



Test Circuit 3. Break-Before-Make Time (t_D)

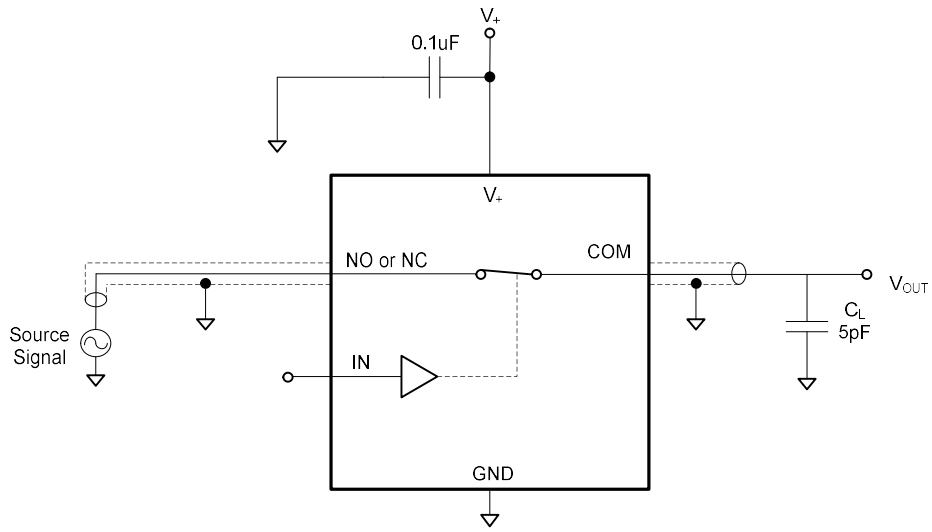


Test Circuit 4. Off Isolation

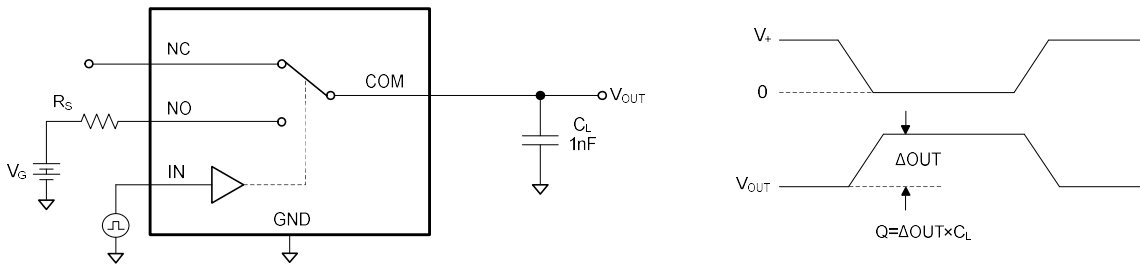


$$\text{Channel To Channel Crosstalk} = 20 \times \log \frac{V_{NO \text{ or } V_{NC}}}{V_{OUT}}$$

Test Circuit 5. Channel-to-Channel Crosstalk



Test Circuit 6. -3dB Bandwidth

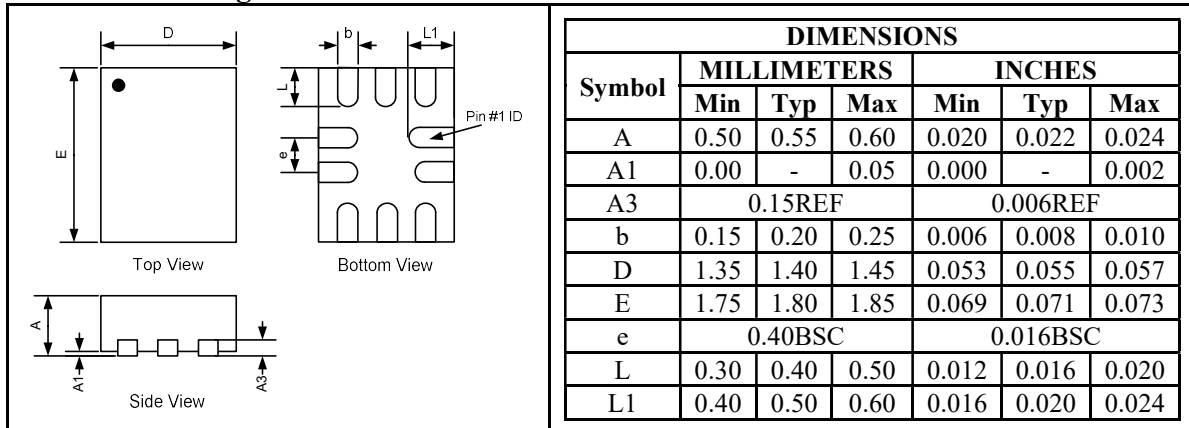


Test Circuit 7. Charge Injection (Q)

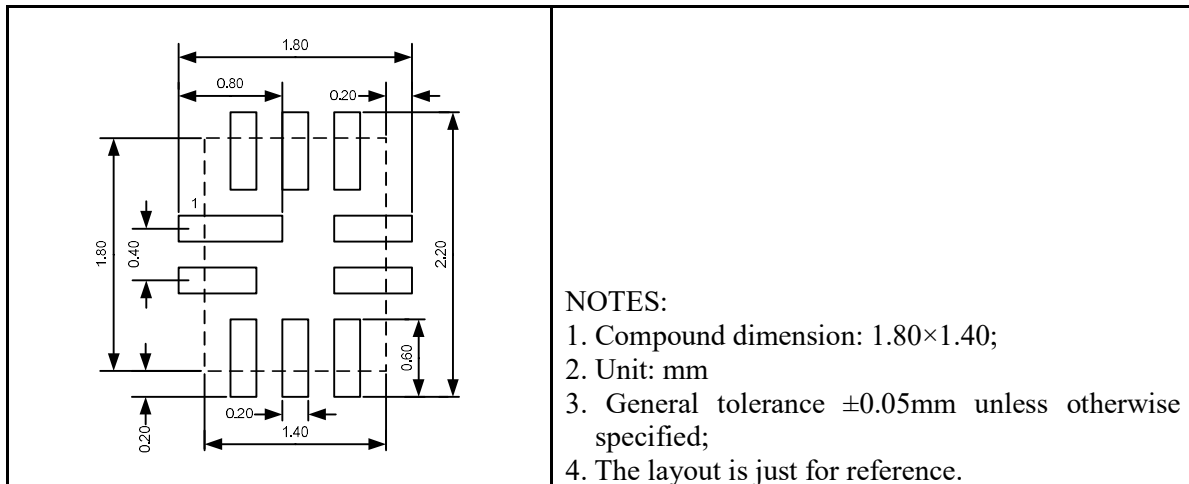
Package Information

UM5223 QFN10 1.8×1.4

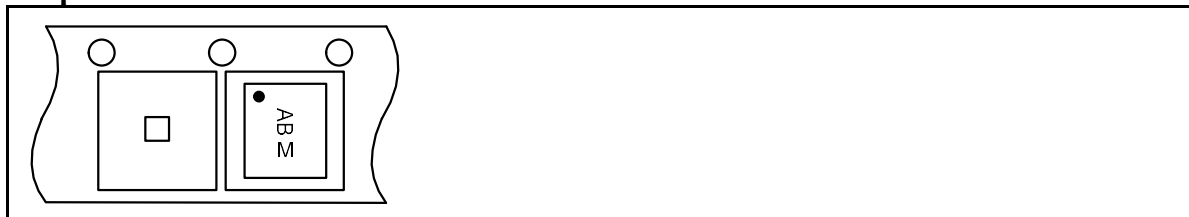
Outline Drawing



Land Pattern



Tape and Reel Orientation



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