1A, 2.5V to 5.5V Input, Low Profile Power Module
UM3503QA QFN24 4.0×4.0

General Description

The UM3503QA is a complete 1A, DC/DC step-down power supply intended for low-power applications. It is capable of delivering 1A output current over a wide input voltage range from 2.5V to 5.5V. Switching regulator, inductor and input/output capacitors are integrated into a tiny 4mm×4mm×1.05mm QFN package. Unless the external resistor divider, no additional components are required to accomplish the design. The UM3503QA is engineered to simplify design and to minimize layout constraints. It is ideal replacement of discrete buck converter to save PCB space.

The UM3503QA is based on a synchronous step-down DC-DC converter optimized for battery-powered portable applications. The DC/DC converter enters the pulse skipping mode automatically at light load condition. This can increase efficiency. The operation frequency is set to 2.25MHz at normal load condition. The UM3503QA enters shutdown mode and consumes less than 1µA when EN pin is pulled low.

The UM3503QA is available in a compact and low profile QFN24 4.0mm×4.0mm×1.05mm package.

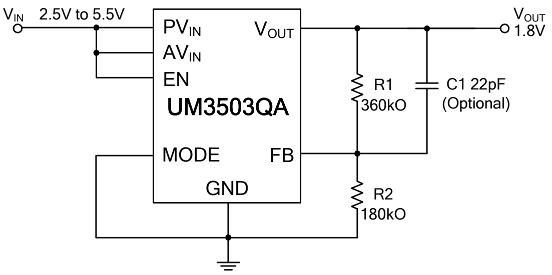
Applications

- LDO Replacement
- FPGA and DSP Point-of-Load Regulator
- Cellular and Smart Phones
- MCU, DSP and FPGA Core Supplies
- Wireless and DSL Modems
- Portable Game Consoles and Instruments
- PDAs, GPS
- Bluetooth Headsets
- Battery-Powered Devices

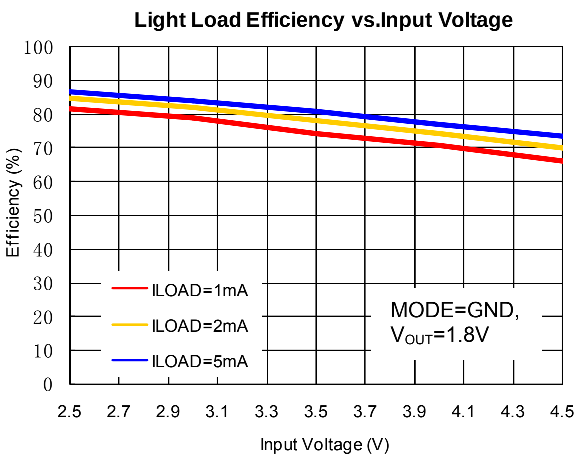
Features

- Ultra Small QFN Package 4.0×4.0×1.05
- High Efficiency: Up to 90%
- 1A Output Current
- 0.6V Minimum Output Voltage
- 2.5V to 5.5V Input Voltage Range
- 2.25MHz Switching Frequency
- 56µA Quiescent Current
- <1µA Shutdown Current
- Excellent Load Transient and Line Transient
- Pulse Skipping Mode Operation
- Low Ripple at Light-Load Pulse Skipping Mode
- Thermal Fault Protection

Typical Application Circuit

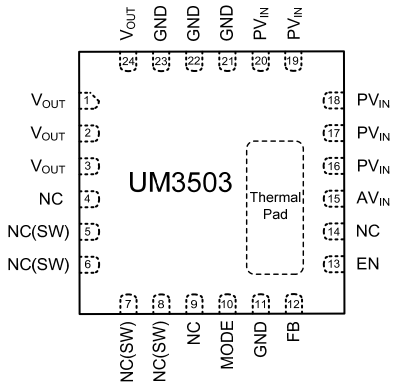


Light Load Efficiency

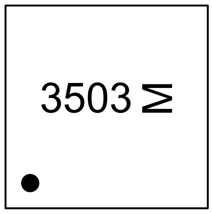


Pin Configurations

(Top View)



Top View



M: Month Code
UM3503QA
QFN24 4.0×4.0

Pin Description

Pin Number	Symbol	Function
1-3, 24	V_{OUT}	Regulated output voltage. They have been connected together inside the chip.
4, 9, 14	NC	Not connected.
5-8	NC(SW)	Not connected—These pins are internally connected to the common switching node of the internal MOSFETs. NC(SW) pins are not to be electrically connected to any external signal, ground, or voltage. However, they must be soldered to the PCB.
10	MODE	MODE pin=high forces the device to operate in fixed-frequency PWM mode. Mode pin=low enables automatic transition from the pulse skipping mode to fixed-frequency PWM mode.
11, 21-23	GND	Ground. They have been connected together inside the chip.
12	FB	Feedback input pin. Connect FB to the center point of the external resistor divider.
13	EN	Regulator enable control input. Pulling this pin to high enables the device. Pulling this pin to low forces the device into shutdown mode. This pin must be terminated.
15	AV_{IN}	Input power supply for the controller circuitry, usually connected to PV_{IN} in the PCB or externally connected to V_{IN} with a decouple capacitor alone.
16-20	PV_{IN}	Input power supply for the MOSFET switches. They have been connected together inside the chip.
-	Thermal Pad	Connected to the ground plane by vias.

Ordering Information

Part Number	Packaging Type	Marking Code	Shipping Qty
UM3503QA	QFN24 4.0×4.0	3503	3000pcs/13Inch Tape & Reel

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Value	Unit
V_{IN}, V_{OUT}	Input and Output Voltages	-0.3 to +6.0	V
V_{EN}, V_{FB}	EN, FB Voltages	-0.3 to V_{IN}+0.3	V
V_{SW}	SW Voltage	-0.3 to V_{IN}+0.3	V
I_O	Peak Output Current	1.2	A
P_D	Continuous Power Dissipation at T_A=25°C	2.31	W
T_O	Operating Temperature	-40 to +85	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_{REFLOW}	Reflow Temperature, MSL3 JEDEC J-STD-020C, 10 Sec	260	°C

Note 1: Stresses greater than those listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Unit
V_{IN}	Input Voltage Range		2.5		5.5	V
V_{OUT}	Output Voltage Range		1		5	V
I_O	Output Current Range		0		1	A
C_{IN}	Additional Output Capacitance	MODE=L		0	10	μF
		MODE=H		0	4.7	μF
C_{OUT}	Additional Output Capacitance	MODE=L		0	10	μF
		MODE=H		0	4.7	μF
C_{FF}	Feedback Capacitance (Optional)			22		pF
R_2	The external resistor to GND		100		300	kΩ
T_A	Ambient Temperature		-40		+85	°C
T_J	Operating Junction Temperature		-40		+125	°C

Electrical Characteristics (Note 2)

(V_{IN}=V_{EN}=3.6V, V_{OUT}=1.8V, T_A=+25°C, no external input/output capacitance, C_{FF}=22pF, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Power						
UVLO	Under Voltage Lockout Threshold		1.8		2.3	V
UVLO_HYS	Under Voltage Lockout Hysteresis			0.2		V
I_Q (Active)	Input DC Supply Current (MODE=L)	I_{LOAD}=0mA		56		µA
	Input DC Supply Current (MODE=H)	I_{LOAD}=0mA		5.6		mA
I_Q (Shutdown)	Input DC Supply Current (Shutdown Mode)	V_{EN}=0V		0.1	1.0	µA
Output						
	Output Voltage Line Regulation	2.5V≤V_{IN}≤5.5V, I_{OUT}=400mA		0.10	0.20	%/V
	Output Voltage Load Regulation	100mA≤I_{OUT}≤1A		0.5		%/A
∆ VO	Ripple Voltage @the pulse skipping mode	I_{OUT}=10mA		35		mV p-p
	Ripple Voltage @the normal mode	I_{OUT}=400mA		4		mV p-p
$R_{DS(ON)}$	Input to Output On-Resistance	100% Duty Cycle I_{OUT}=1A		500		mΩ
t_{SS}	Soft Start Time			400		µs
$\eta_{(max)}$	Efficiency @the pulse skipping mode	I_{OUT}=1mA		78		%
	Efficiency @the pulse skipping mode	I_{OUT}=10mA		83		
	Efficiency @ Light Load	I_{OUT}=100mA		86		
	Efficiency @ middle Load	I_{OUT}=400mA		85		
FB						
V_{FB}	Feedback Voltage	T_A=25°C	0.588	0.6000	0.612	V
		T_A=-40~85°C	0.5830	0.6000	0.6150	
I_{FB}	FB Input Bias Current	V_{FB}=0.65V			30	nA
MODE,EN						
V_H	MODE EN High-Level Threshold		1.2			V
V_L	MODE EN Low-Level Threshold				0.4	V
I_L	MODE Leakage Current			±0.1	±1	µA
Oscillator						
f	PFM Oscillator Frequency	V_{FB}=0.6V or V_{OUT}=100%	1.95	2.25	2.55	MHz

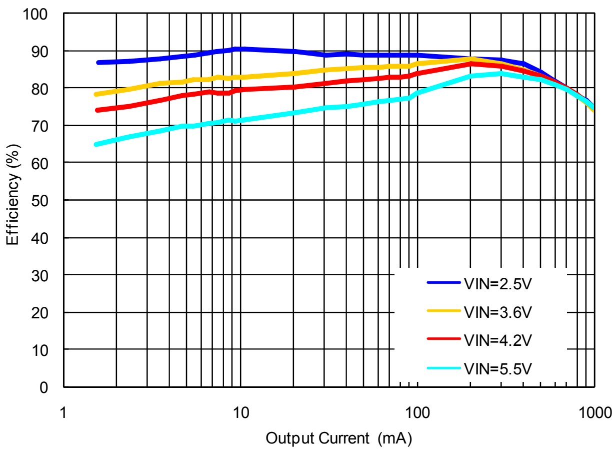
Protection						
I_{LIM}	Peak Input Current Limit			1.5		A
	Thermal Shutdown Temperature			160		ºC
	Thermal Shutdown Trip Point Hysteresis			25		ºC

Note 2: 100% production test at +25ºC. Specifications over the temperature range are guaranteed by design and characterization.

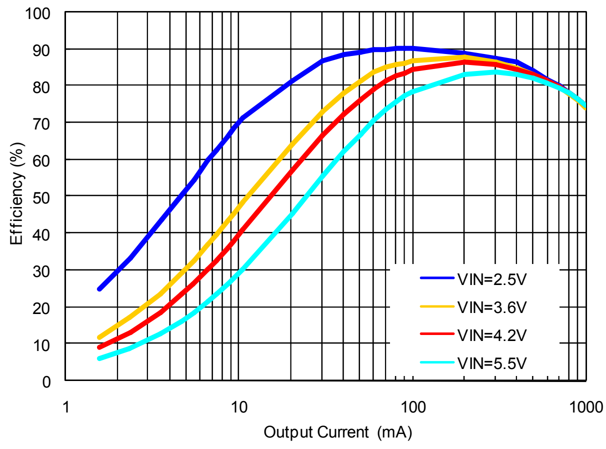
Typical Operating Characteristics

(V_{IN}=3.6V, V_{OUT}=1.8V, no external input/output capacitance, C_{FF}=22pF, T_A=+25°C, unless otherwise noted.)

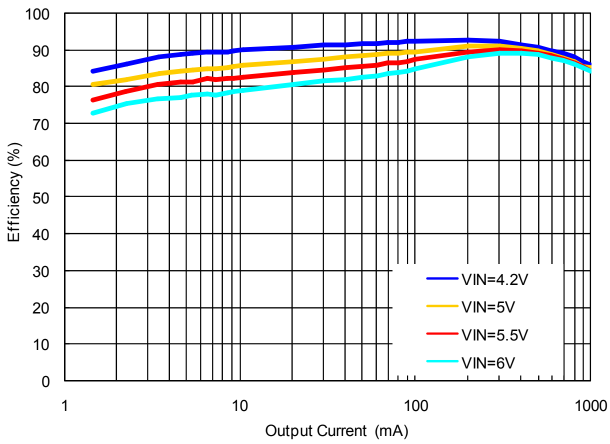
Efficiency vs. Load Current
V_{OUT}=1.8V, Power Save Mode



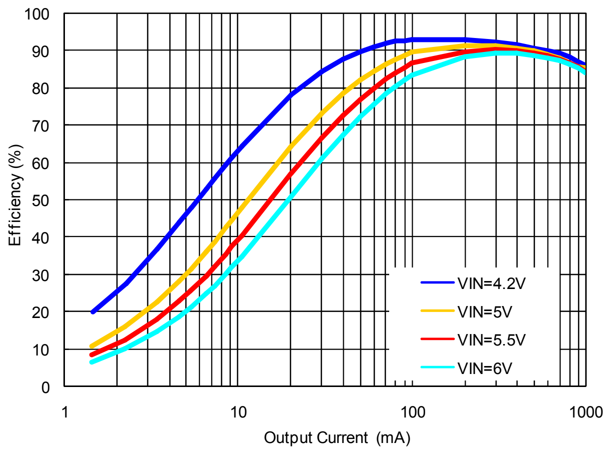
Efficiency vs. Load Current
V_{OUT}=1.8V, Forced PWM Mode



Efficiency vs. Load Current
V_{OUT}=3.3V, Power Save Mode



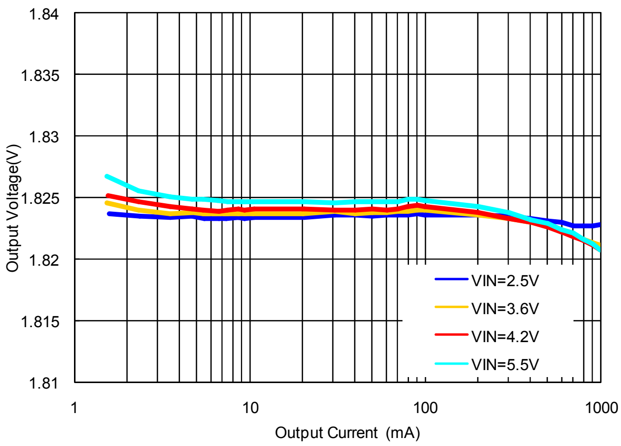
Efficiency vs. Load Current
V_{OUT}=3.3V, Forced PWM Mode



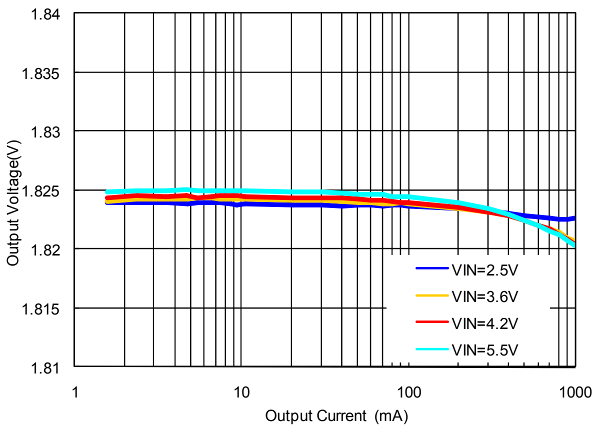
Typical Operating Characteristics (Continued)

(V_{IN}=3.6V, V_{OUT}=1.8V, no external input/output capacitance, C_{FF}=22pF, T_A=+25°C, unless otherwise noted.)

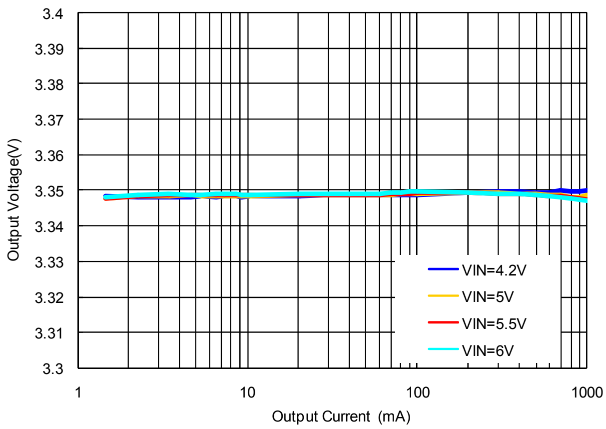
Output Voltage vs. Load Current
V_{OUT}=1.8V, MODE=L



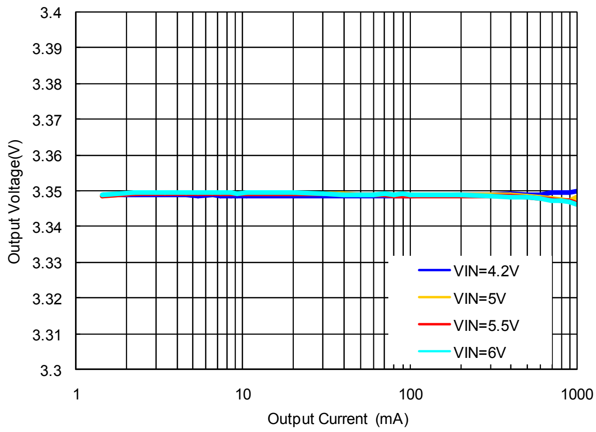
Output Voltage vs. Load Current
V_{OUT}=1.8V, MODE=H



Output Voltage vs. Load Current
V_{OUT}=3.3V, MODE=L

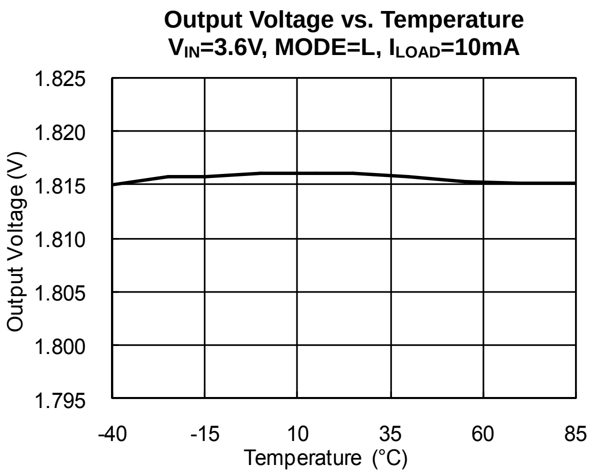


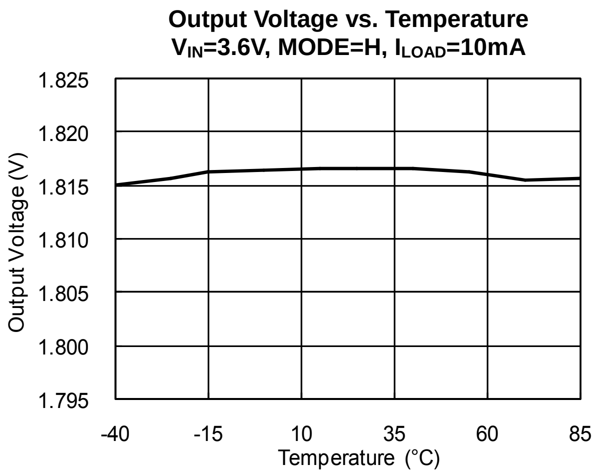
Output Voltage vs. Load Current
V_{OUT}=3.3V, MODE=H

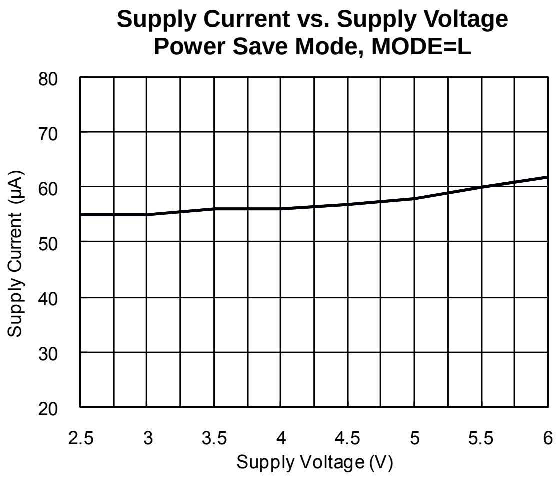


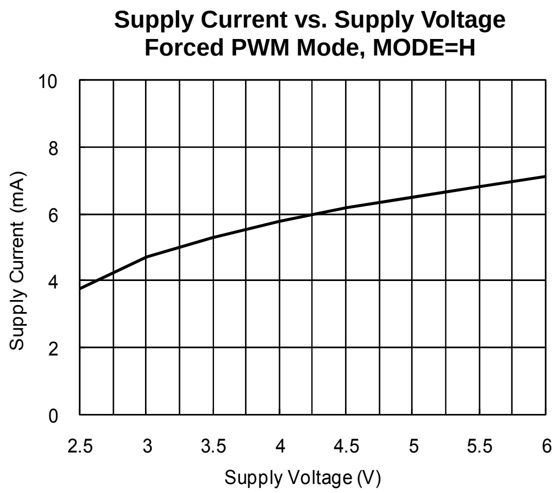
Typical Operating Characteristics (Continued)

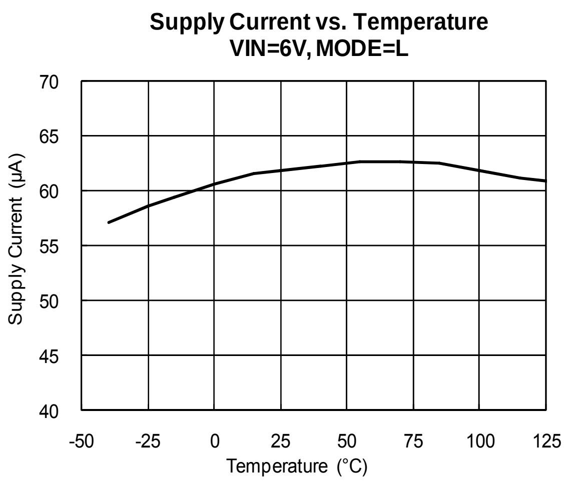
(V_{IN}=3.6V, V_{OUT}=1.8V, no external input/output capacitance, C_{FF}=22pF, T_A=+25°C, unless otherwise noted.)

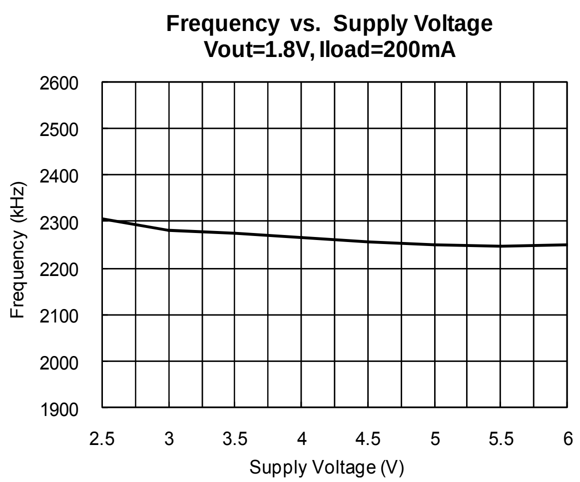








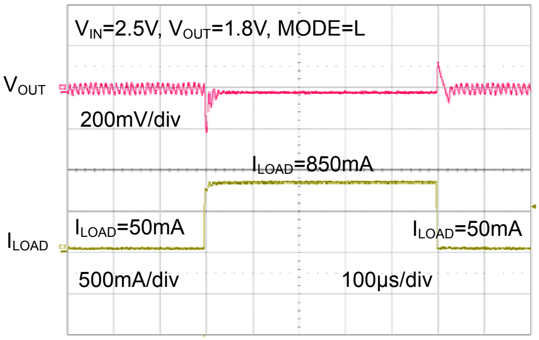




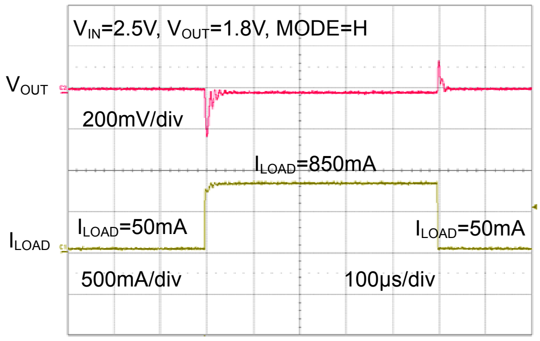
Typical Operating Characteristics (Continued)

(V_{IN}=3.6V, V_{OUT}=1.8V, no external input/output capacitance, C_{FF}=22pF, T_A=+25°C, unless otherwise noted.)

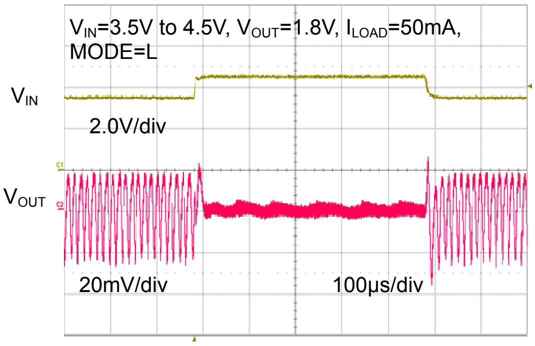
Load Transient Response



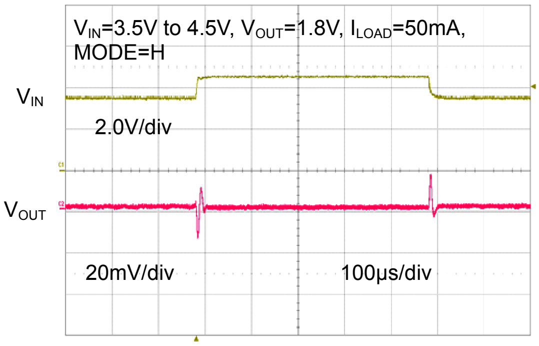
Load Transient Response



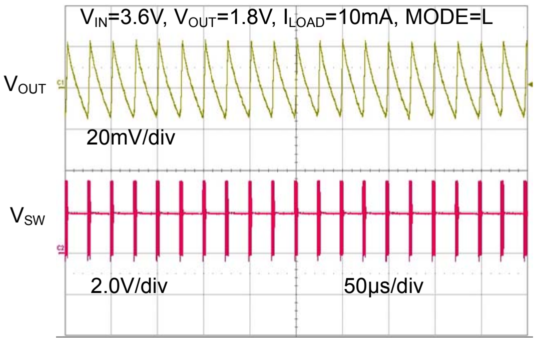
Line Transient Response



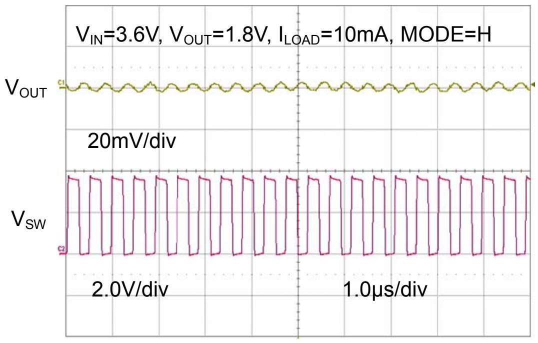
Line Transient Response



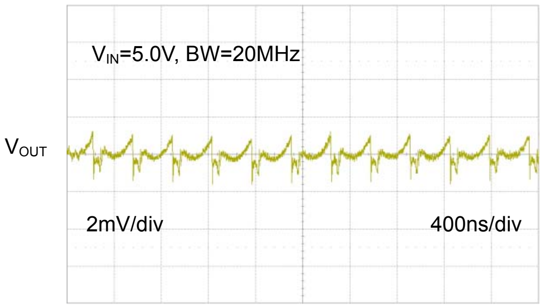
PFM Mode Operation



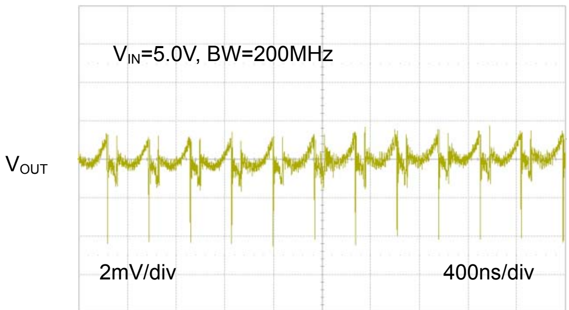
PWM Mode Operation



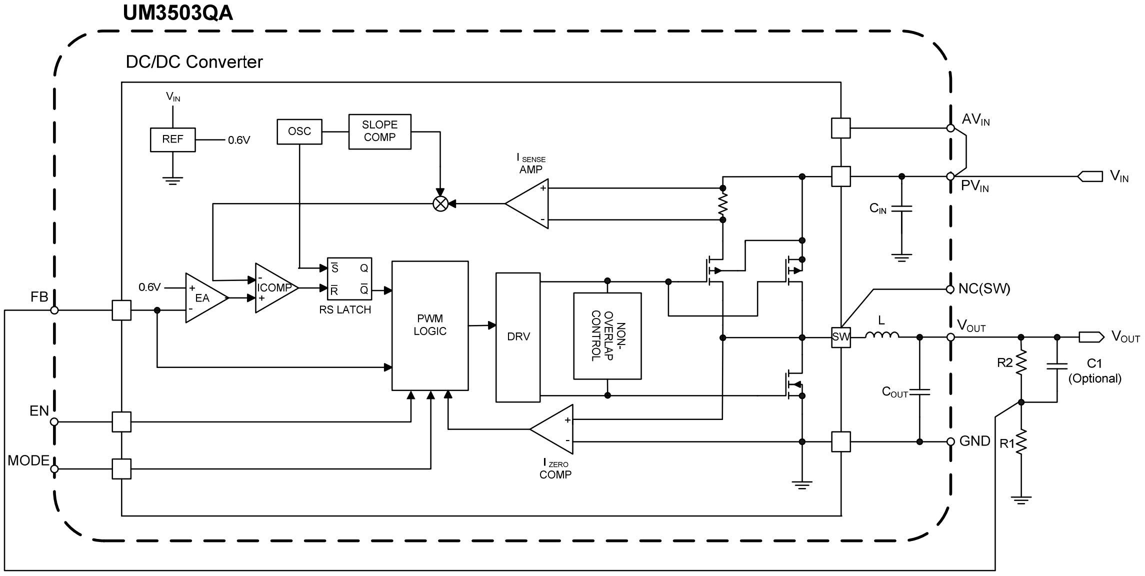
Ripple and HF Noise (I_{OUT}=300mA)



Ripple and HF Noise (I_{OUT}=300mA)



Block Diagram



Function Description

Operation

The UM3503QA is a complete 1A, DC/DC step-down power supply converter. Switching regulator, inductor and input/output capacitors are integrated into a tiny QFN package. No additional components are required to finish the design.

At light load currents, the UM3503QA operates in a pulse skipping mode. At normal load, it operates in a fixed frequency mode. Combined with good load and line transient response characteristics, the low quiescent current (typical 56μA) allows the device to maintain high efficiency at light load, while preserving fast transient response for applications.

The UM3503QA integrates an input current limit to protect the device against heavy load or short circuits and features an undervoltage lockout circuit to prevent the device from misoperation at low input voltages.

Pulse Skipping Mode Operation

At very light loads, the UM3503QA automatically enters Pulse Skipping Mode. In the Pulse Skipping Mode, the inductor current may reach zero or reverse on each pulse. The PWM control loop will automatically skip pulses to maintain output regulation. The bottom MOSFET is turned off by the current reversal comparator, I_{ZERO}, and the switch voltage will ring. This is discontinuous mode operation and is normal behavior for the switching regulator.

Mode Selection

The MODE pin allows selection of the operating mode of the device. Connecting this pin to GND enables the automatic PWM and pulse skipping mode operation. The converter operates in regulated frequency PWM mode at moderate to heavy loads and in the pulse skipping mode during light loads, which maintains high efficiency over a wide load current range.

Pulling the MODE pin high forces the converter to operate in the PWM mode even at light load currents. The advantage is that the converter operates with a fixed frequency that allows simple filtering of the switching frequency for noise-sensitive applications. In this mode, the efficiency is lower compared to the power save mode during light loads.

Low Dropout, 100% Duty Cycle Operation

The device starts to enter 100% duty cycle mode once the input and output voltage come close together. In order to maintain the output voltage, the DC/DC converter's high-side MOSFET is turned on 100% for one or more cycles.
With further decreasing V_{IN}, the high-side switch is constantly turned on, thereby providing a low input-to-output voltage difference. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantages of the whole battery voltage range.

Soft Start

The UM3503QA has an internal soft-start circuit that limits the inrush current during start-up. This limits input voltage drops when a battery or a high-impedance power source is connected to the input. This mode of operation continues for typical 400µs after enable.

Enable

The EN pin provides a means to shut down the converter or enable normal operation. A logic low will disable the converter and cause it into shut down. A logic high will enable the converter into normal operation. In shutdown mode, the quiescent current of the device will be less than 1µA. The EN pin must not be left floating.

Input Capacitor Selection

Because of the pulsating input current nature of the buck converter, a low ESR input capacitor is required to prevent large voltage transients that can cause misbehavior of the device or interference in other circuits in the system.
For most applications, the input capacitor that is integrated into the UM3503QA should be sufficient. If the application exhibit a noisy or erratic switching frequency, experiment with additional input ceramic capacitor to find a remedy.
The UM3503QA uses a tiny ceramic input capacitor. When a ceramic capacitor is combined with trace or cable inductance, such as from a wall adapter, a load step at the output can induce ringing at the V_{IN} pin. This ringing can couple to the output and be mis-treated as loop instability or can even damage the part. In this circumstance, an additional "bulk" capacitor, such as electrolytic or tantalum, should be placed between the input of the converter and the power source. This will lead to reducing ringing that may occur between the inductance of the power source leads and C_{IN}.

Output Capacitor Selection

The advanced, fast-response, current mode control scheme of the UM3503QA allows the use of a tiny ceramic output capacitor (C_{OUT}). For most applications, the output capacitor integrated in the UM3503QA is sufficient.
At normal load current, the device operates in PWM mode; the overall output voltage ripple is the sum of the voltage step that is caused by the output capacitor ESL and the ripple current that flows through the output capacitor impedance. At light loads, the output capacitor limits the output ripple voltage and provides holdup during large load transitions.
The UM3503QA is designed as a Point-Of-Load (POL) regulator, to operate stand-alone without requiring any additional capacitance. Adding a 10µF ceramic output capacitor (X7R or X5R dielectric) generally works from a converter stability point of view, helps to minimize the output ripple voltage in pulse skipping mode and improves the converter's transient response when input and output voltage are close together.

Thermal Shutdown

When excessive power is dissipated in the chip, the junction temperature rises. Once the junction temperature exceeds the thermal shutdown temperature, the thermal shutdown circuit turns off the converter output voltage thus allowing the device to cool. When the junction temperature decreases by 25°C, the device will go through the normal startup process.

Applications Information

Output Voltage Setting

The output voltage can be caculated according to the formula below with an internal reference volatge V_{REF} typical 0.6V:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

To minimize the current through the feedback divider network, the recommended value of R2 is about 180kΩ. The sum of R1 and R2 should not exceed about 1MΩ to keep the network robust against noise. An external feed forward capacitor C1 is required for optimum load transient response. The value of C1 should be in the range between 10pF and 33pF.
Route the FB line away from noise sources, such as the inductor or the SW line.

Exposed Metal on the Bottom of the Package

The UM3503QA utilizes the lead frame as part of the electrical circuit. The lead frame offers many advantages in thermal performance, in reduced electrical lead resistance and in overall foot print. However, it does require some special considerations.
As part of the package assembly process, lead frame construction requires for mechanical support, some of the lead-frame metal is exposed at the point where wire-bond or internal passives are attached. This results in several small pads being exposed on the bottom of the package.
The "grayed-out" area in Figure 1 represents the area that should be clear of any metal (traces, vias, or planes) on the top layer of the PCB. The exposed thermal pad should be connected to the ground plane by vias for better thermal performance.

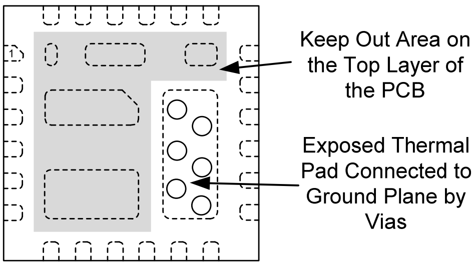


Figure 1. Exposed Metal of the Package

Layout Guidance

The package of the UM3503QA has been optimized that makes it easy for layout. It is an ideal choice to be used to replace less efficient LDO to achieve improved efficiency in space restricted applications.
When laying out the PC board, the following suggestions should be taken to ensure higher performance of the UM3503QA.

1. PCB with at least two planes is recommended. Keep the GND plane under the converter as complete as possible.
2. Although C_{IN} and C_{OUT} have been integrated inside the chip, additional input and output capacitors can also be added to achieve better performance. Please connect the additional input capacitor to the PV_{IN} and GND pins, the additional output capacitor to the V_{OUT} and GND pins as closely as possible to get good power filter effect.
3. The power traces, including the GND trace, the PV_{IN} trace and V_{OUT} trace should be kept short, direct and wide to allow large current flow.
4. The AV_{IN} pin is usually connected to PV_{IN} in the PCB or externally connected to V_{IN} with

a decouple capacitor alone. A 0.1μF capacitor can be used to decouple for better performance.

5. Keep the SW pin away from the sensitive FB node. This pin should also not be electrically connected to any external signal, ground, or voltage.
6. Do not trace signal line under the chip.
7. For better thermal performance, the exposed thermal pad should be connected to the groud plane by vias.

The recommended layout is shown below in Figure 2.

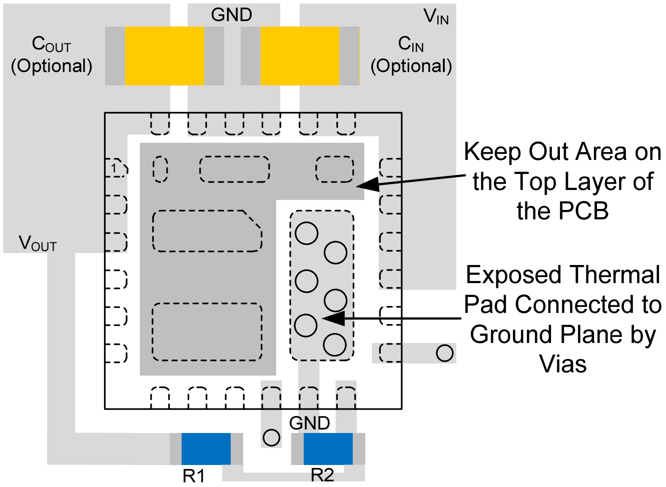
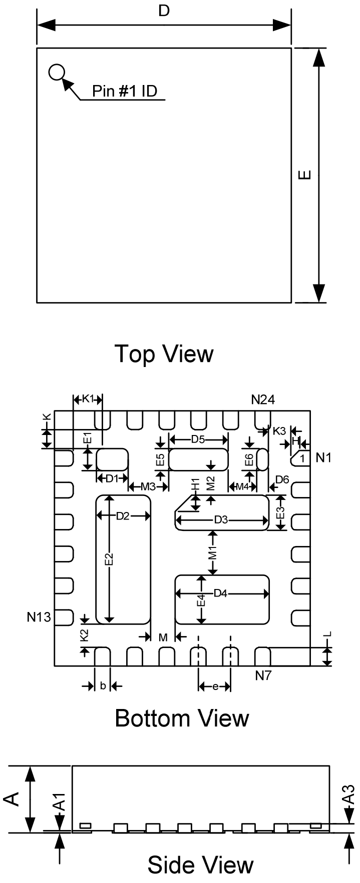


Figure 2. Layout Recommendation

Package Information

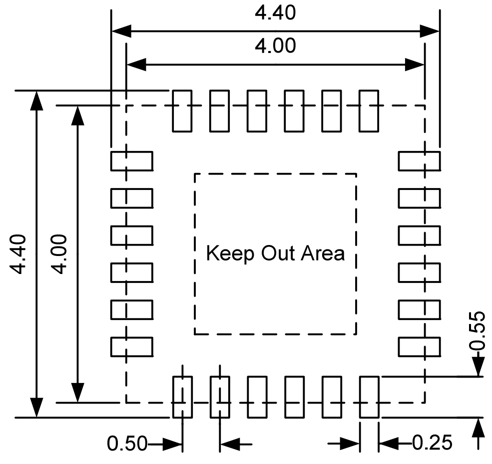
UM3503QA: QFN24 4.0×4.0

Outline Drawing



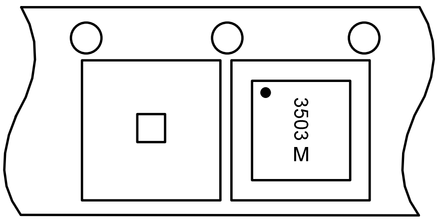
Symbol	DIMENSIONS					
	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	1.00	1.05	1.10	0.039	0.041	0.043
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.152REF			0.006REF		
b	0.20	0.25	0.30	0.008	0.010	0.012
D	3.90	4.00	4.10	0.154	0.157	0.161
E	3.90	4.00	4.10	0.154	0.157	0.161
D1	0.40	0.50	0.60	0.016	0.020	0.024
E1	0.25	0.35	0.45	0.010	0.014	0.018
D2	0.75	0.85	0.95	0.030	0.033	0.037
E2	1.92	2.02	2.12	0.076	0.080	0.083
D3	1.37	1.47	1.57	0.054	0.058	0.062
E3	0.45	0.55	0.65	0.018	0.022	0.026
D4	1.37	1.47	1.57	0.054	0.058	0.062
E4	0.67	0.77	0.87	0.026	0.030	0.034
D5	0.84	0.94	1.04	0.033	0.037	0.041
E5	0.25	0.35	0.45	0.010	0.014	0.018
D6	0.10	0.20	0.30	0.004	0.008	0.012
E6	0.25	0.35	0.45	0.010	0.014	0.018
e	0.40	0.50	0.60	0.016	0.020	0.024
H	0.125REF			0.005REF		
H1	0.25REF			0.010REF		
K	0.20	0.30	0.40	0.008	0.012	0.016
K1	0.25	0.35	0.45	0.010	0.014	0.018
K2	0.25	0.35	0.45	0.010	0.014	0.018
K3	0.25	0.35	0.45	0.010	0.014	0.018
L	0.25	0.30	0.35	0.010	0.012	0.014
M	0.28	0.38	0.48	0.011	0.015	0.019
M1	0.60	0.70	0.80	0.024	0.028	0.031
M2	0.28	0.38	0.48	0.011	0.015	0.019
M3	0.53	0.63	0.73	0.021	0.025	0.029
M4	0.33	0.43	0.53	0.013	0.017	0.021

Land Pattern



NOTES:
1. Compound dimension: 4.00×4.00;
2. Unit: mm;
3. General tolerance ±0.05mm unless otherwise specified;
4. The layout is just for reference.

Tape and Reel Orientation



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http://www.union-ic.com/index.aspx?cat_code=RoHSDeclaration

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Union Semiconductor, Inc

Add: Unit 606, No.570 Shengxia Road, Shanghai 201210

Tel: 021-51093966

Fax: 021-51026018

Website: www.union-ic.com