3-V LVDS Quad CMOS Differential Line Driver

UM3404SG ***SOP16***
UM3404UG ***TSSOP16***

1 Description

The UM3404 is a quad CMOS differential line driver designed for applications requiring ultra low power dissipation and high data rates. The device is designed to support data rates in excess of 400 Mbps (200 MHz) using Low Voltage Differential Signaling (LVDS) technology.

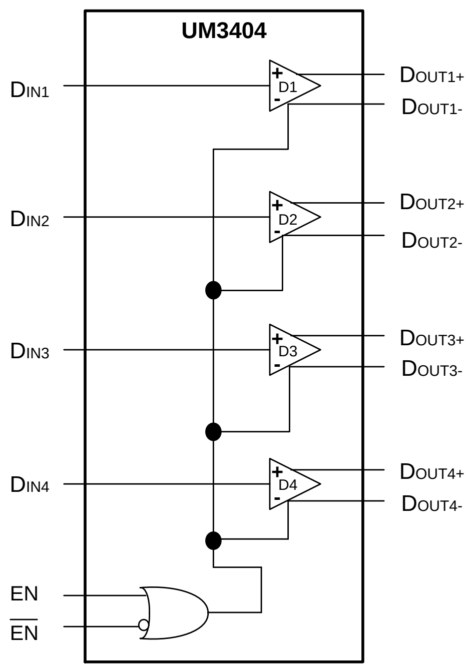
The UM3404 accepts low voltage LVTTL or LVCMOS input levels and translates them to low voltage (350 mV) differential output signals. In addition the driver supports a TRI-STATE function that may be used to disable the output stage, disabling the load current, and thus dropping the device to an ultra low idle power state of 13 mW typical.

The EN and $\overline{\text{EN}}$ inputs allow active Low or active High control of the TRI-STATE outputs. The enables are common to all four drivers. The UM3404 and companion line receiver (UM3403) provide a new alternative to high power psuedo-ECL devices for high speed point-to-point interface applications.

2 Applications

- Building And Factory Automation
- Grid Infrastructure

Block Diagram



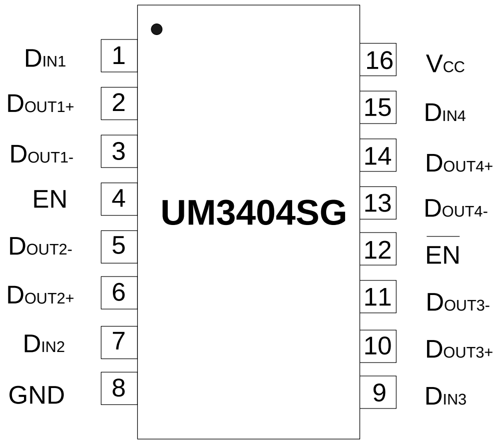
3 Features

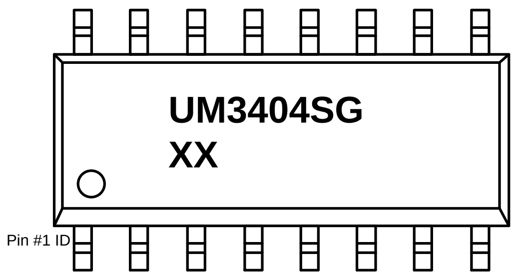
- >400Mbps (200MHz) Switching Rates
- 0.1-ns Typical Differential Skew
- 0.4-ns Maximum Differential Skew
- 2-ns Maximum Propagation Delay
- 3.3-V Power Supply Design
- ±350-mV Differential Signaling
- Low Power Dissipation (13-mW at 3.3-V Static)
- Interoperable With Existing 5-V LVDS Devices
- Compatible With IEEE 1596.3 SCI LVDS Standard
- Compatible With TIA/EIA-644 LVDS Standard
- Industrial Operating Temperature Range
- Available in SOP and TSSOP Surface-Mount Packaging

4 Ordering Information

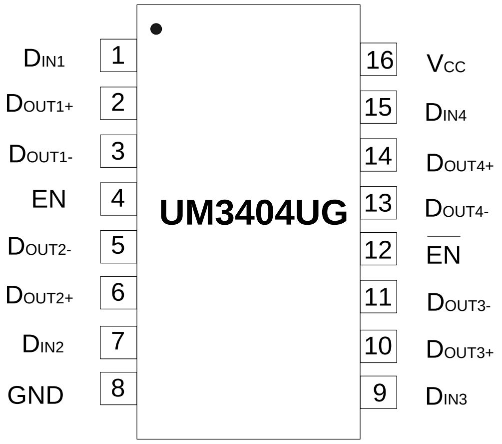
Part Number	Marking Code	Package Type	Shipping Qty
UM3404SG	UM3404SG	SOP16	2500pcs/13 Inch Tape & Reel
UM3404UG	UM3404UG	TSSOP16	3000pcs/13 Inch Tape & Reel

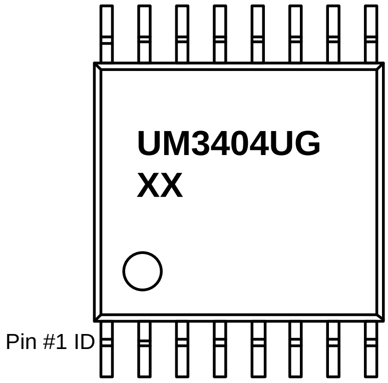
5 Pin Configuration and Function





XX: Week Code
UM3404SG
SOP16





XX: Week Code
UM3404UG
TSSOP16

Table 5-1. Pin Functions

Pin No.	Pin Name	Function
1	D_{IN1}	Driver input pin, TTL/CMOS compatible
2	D_{OUT1+}	Noninverting driver output pin, LVDS levels
3	D_{OUT1-}	Inverting driver output pin, LVDS levels
4	EN	Active high enable pin, OR-ed with $\overline{EN}$
5	D_{OUT2-}	Inverting driver output pin, LVDS levels
6	D_{OUT2+}	Noninverting driver output pin, LVDS levels
7	D_{IN2}	Driver input pin, TTL/CMOS compatible
8	GND	Ground pin
9	D_{IN3}	Driver input pin, TTL/CMOS compatible
10	D_{OUT3+}	Noninverting driver output pin, LVDS levels
11	D_{OUT3-}	Inverting driver output pin, LVDS levels
12	$\overline{EN}$	Active low enable pin, OR-ed with EN
13	D_{OUT4-}	Inverting driver output pin, LVDS levels
14	D_{OUT4+}	Noninverting driver output pin, LVDS levels
15	D_{IN4}	Driver input pin, TTL/CMOS compatible
16	V_{CC}	Power supply pin, 3.3 V ±0.3 V

6 Specifications

6.1 Recommended Operating Conditions

Symbol	Parameter	MIN	NOM	MAX	Unit
V_{CC}	Supply Voltage	3	3.3	3.6	V
T_A	Operating free-air temperature	-40	25	85	℃

6.2 Absolute Maximum Ratings (Note 1)

Over operating free-air temperature range(unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage		-0.3		4	V
V_I	Input Voltage		-0.3		V_{CC}+0.3	V
$V_{EN/\overline{EN}}$	Enable input voltage		-0.3		V_{CC}+0.3	V
V_{DOUT+}/ V_{DOUT-}	Output voltage		-0.3		3.9	V
I_{DOUT+}/ I_{DOUT-}			Continuous			
V_{ESD}	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001	Note 2		±6		kV
T_{STG}	Storage Temperature Range		-65		150	℃
T_L	Lead Temperature for Soldering 10 seconds				260	℃
	Maximum junction temperature				150	℃

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
Note 2: JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Thermal Information

Symbol	Parameter	SOP16	TSSOP16	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	75	114	℃/W
$R_{\theta JC}$	Junction-to-case (top) thermal resistance	36	51	℃/W
$R_{\theta JA}$	Junction-to-board thermal resistance	32	59	℃/W
$\psi_{\theta JT}$	Junction-to-top characterization parameter	6	8	℃/W
$\psi_{\theta JB}$	Junction-to-board characterization parameter	31.7	58	℃/W

6.4 Electrical Characteristics (Static) (Note 1, 2, 3)

over supply voltage and operating temperature ranges (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OD1}	Differential output voltage	R_L=100Ω, D_{OUT-}, D_{OUT+} pins,See Figure 7-1	250	350	450	mV
Δ V_{OD1}	Change in magnitude of V_{OD1} for complementary output states	R_L=100Ω, D_{OUT-}, D_{OUT+} pins, See Figure 7-1		4	35	|mV|
V_{OS}	Offset voltage	R_L=100Ω, D_{OUT-}, D_{OUT+} pins, See Figure 7-1	1.125	1.25	1.375	V
Δ V_{OS}	Change in magnitude of V_{OS} for complementary output states	R_L=100Ω, D_{OUT-}, D_{OUT+} pins, See Figure 7-1		5	25	|mV|
V_{OH}	Output voltage high	R_L=100Ω, D_{OUT-}, D_{OUT+} pins, See Figure 7-1		1.38	1.6	V
V_{OL}	Output voltage low	R_L=100Ω, D_{OUT-}, D_{OUT+} pins, See Figure 7-1	0.9	1.03		V
V_{IH}	Input voltage high	D_{IN}, EN, $\overline{EN}$ pins	2		V_{CC}	V
V_{IL}	Input voltage low	D_{IN}, EN, $\overline{EN}$ pins	0		0.8	V
V_{CL}	Input clamp voltage	I_{CL} = -18 mA, D_{IN}, EN, $\overline{EN}$ pins	-1.5	-0.8		V
I_{OS}	Output short circuit current	Enabled, D_{OUT-}, D_{OUT+} pins, D_{IN}= V_{CC}, D_{OUT+}= 0V,or D_{IN} = GND, D_{OUT-}= 0V (Note 4)		-6	-9	mA
I_{OSD}	Differential output short circuit current	Enabled, V_{OD} = 0 V, D_{OUT-}, D_{OUT+} pins (Note 4)		-6	-9	mA
I_{OFF}	Power-off leakage	V_{OUT} = 0 V or 3.6 V, V_{CC} = 0 V or open, D_{OUT-}, D_{OUT+} pins	-20	±1	20	μA
I_{OZ}	Output TRI-STATE current	EN = 0.8 V and $\overline{EN}$= 2 V, V_{OUT} = 0 V or V_{CC}, D_{OUT-}, D_{OUT+} pins	-10	±1	10	μA

6.4 Electrical Characteristics (Static)---continued (Note 1, 2, 3)

over supply voltage and operating temperature ranges (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	No load supply current drivers enabled	D_{IN} = V_{CC} or GND, V_{CC} pin		5	8	mA
I_{CCL}	Loaded supply current drivers enabled	R_L = 100 Ω (all channels), D_{IN} = V_{CC} or GND (all inputs), V_{CC} pin		23	30	mA
I_{CCZ}	No load supply current drivers disabled	D_{IN} = V_{CC} or GND, $\overline{EN}$ = V_{CC}, EN = GND, V_{CC} pin		2.6	6	mA

Note 1: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except: V_{OD1} and ΔV_{OD1}.
Note 2: All typicals are given for: V_{CC} = 3.3 V, T_A = 25 ℃.
Note 3: The UM3404 is a current mode device and only functions within datasheet specifications when a resistive load is applied to the driver outputs typical range is (90 Ω to 110 Ω)
Note 4: Output short-circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

6.5 Electrical Characteristics (Dynamic) (Note 1, 2, 3)

V_{CC} = 3.3 V ±10% and T_A = -40 ℃ to 85 ℃(unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PHLD}	Differential Propagation delay high to low	R_L=100Ω, C_L=10pF See Figure 7-2 and Figure 7-3	0.8	1.18	2	ns
t_{PLHD}	Differential Propagation delay low to high	R_L=100Ω, C_L=10pF See Figure 7-2 and Figure 7-3	0.8	1.25	2	ns
t_{SKD1}	Differential pulse skew, $\|t_{PHLD}-t_{PLHD}\|$	R_L=100Ω, C_L=10pF See Figure 7-2 and Figure 7-3 (Note 4)	0	0.07	0.4	ns
t_{SKD2}	Channel-to-channel skew	R_L=100Ω, C_L=10pF See Figure 7-2 and Figure 7-3 (Note 5)	0	0.1	0.5	ns
t_{SKD3}	Differential part-to-part skew	R_L=100Ω, C_L=10pF See Figure 7-2 and Figure 7-3 (Note 6)	0		1	ns
t_{SKD4}	Differential part-to-part skew	R_L=100Ω, C_L=10pF See Figure 7-2 and Figure 7-3 (Note 7)	0		1.2	ns
t_{TLH}	Rise time	R_L=100Ω, C_L=10pF See Figure 7-2 and Figure 7-3		0.38	1.5	ns
t_{THL}	Fall time	R_L=100Ω, C_L=10pF See Figure 7-2 and Figure 7-3		0.4	1.5	ns
t_{PHZ}	Disable time high to Z	R_L=100Ω, C_L=10pF See Figure 7-4 and Figure 7-5			5	ns
t_{PLZ}	Disable time low to Z	R_L=100Ω, C_L=10pF See Figure 7-4 and Figure 7-5			5	ns
t_{PZH}	Enable time Z to high	R_L=100Ω, C_L=10pF See Figure7- 4 and Figure 7-5			7	ns
t_{PZL}	Enable time Z to low	R_L=100Ω, C_L=10pF See Figure 7-4 and Figure 7-5			7	ns

6.5 Electrical Characteristics (Dynamic)---continued (Note 1, 2, 3)

V_{CC} = 3.3 V ±10% and T_A = -40 ℃ to 85 ℃(unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{MAX}	Maximum operating frequency	Note 8	200	250		MHz

Note 1: All typicals are given for: V_{CC} = 3.3 V, T_A = 25 ℃.
Note 2: Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z_O = 50 Ω, $t_r \leq 1$ ns, and $t_f \leq 1$ ns.
Note 3: C_L includes probe and jig capacitance.
Note 4: t_{SKD1}, $|t_{PHLD} - t_{PLHD}|$ is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
Note 5: t_{SKD2} is the differential channel-to-channel skew of any event on the same device.
Note 6: t_{SKD3}, differential part-to-part skew, is defined as the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same VCC and within 5 ℃ of each other within the operating temperature range.
Note 7: t_{SKD4}, part-to-part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. t_{SKD4} is defined as |Max − Min| differential propagation delay.
Note 8: f_{MAX} generator input conditions: $t_r = t_f < 1$ ns, (0% to 100%), 50% duty cycle, 0 V to 3 V. Output criteria: duty cycle = 45% / 55%, V_{OD} > 250 mV, all channels switching

7 Parameter Measurement Information

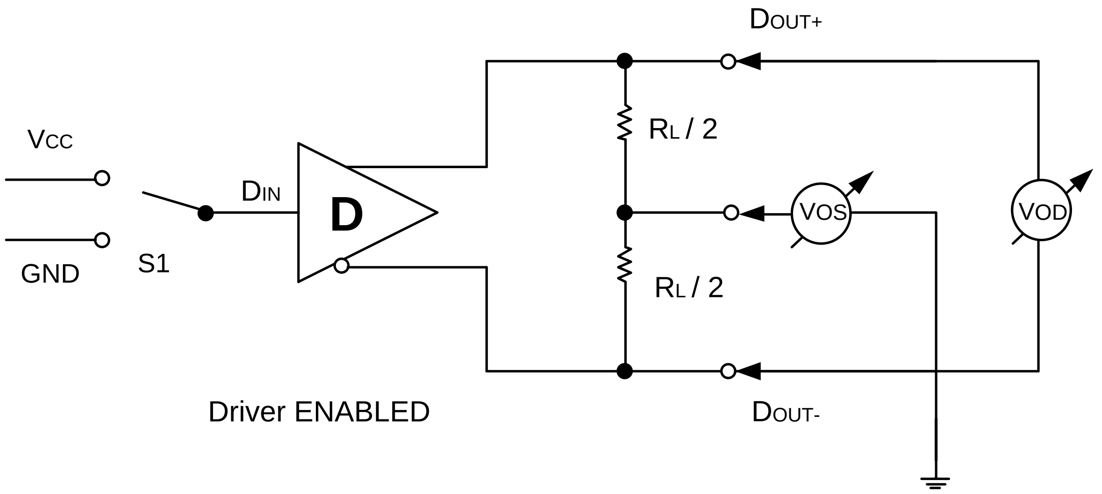


Figure 7-1. Driver V_{OD} and V_{OS} Test Circuit

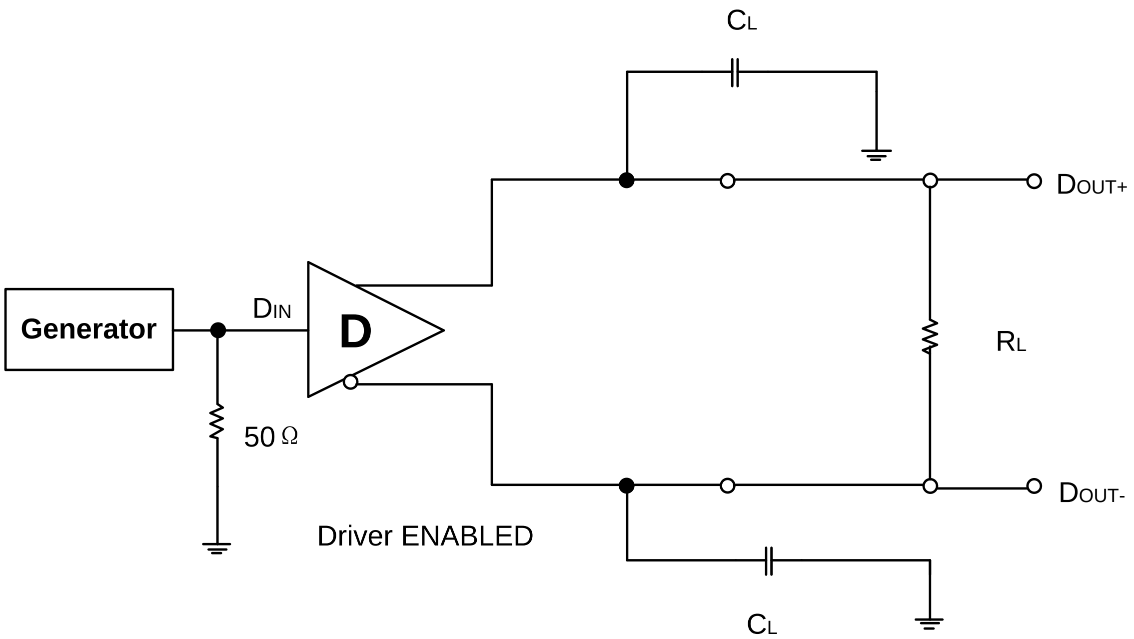


Figure 7-2. Driver Propagation Delay and Transition Time Test Circuit

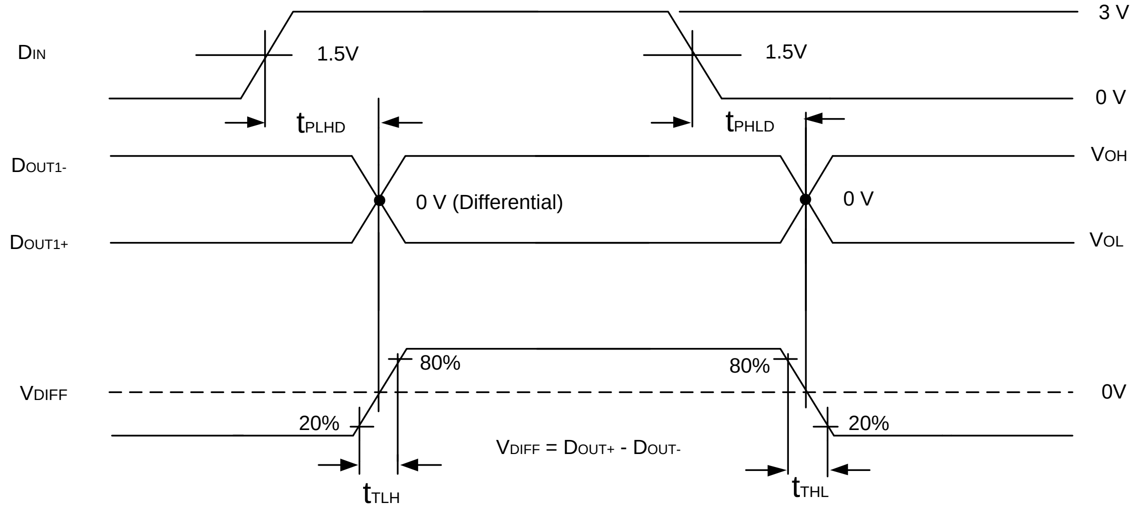


Figure 7-3. Driver Propagation Delay and Transition Time Waveforms

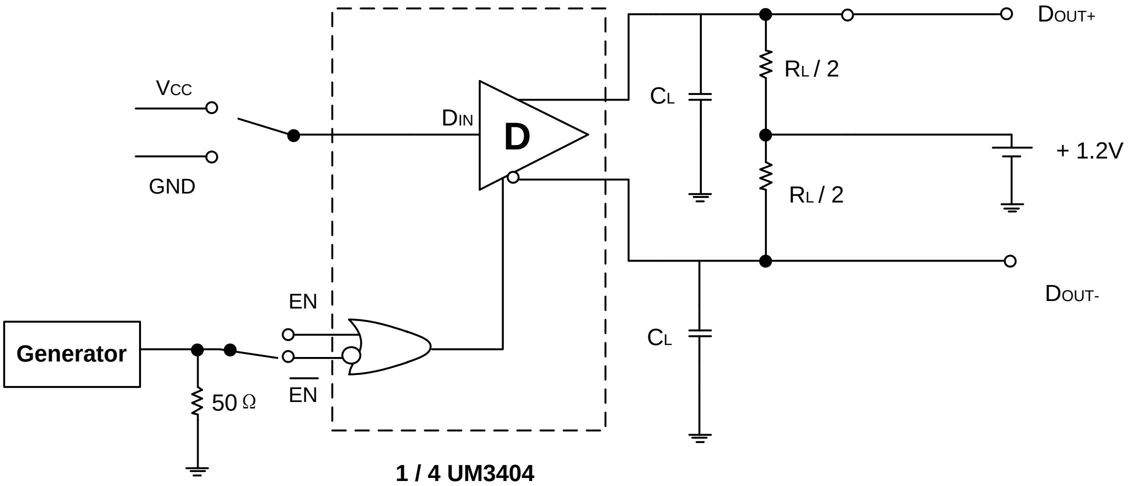


Figure 7-4. Driver TRI-STATE Delay Test Circuit

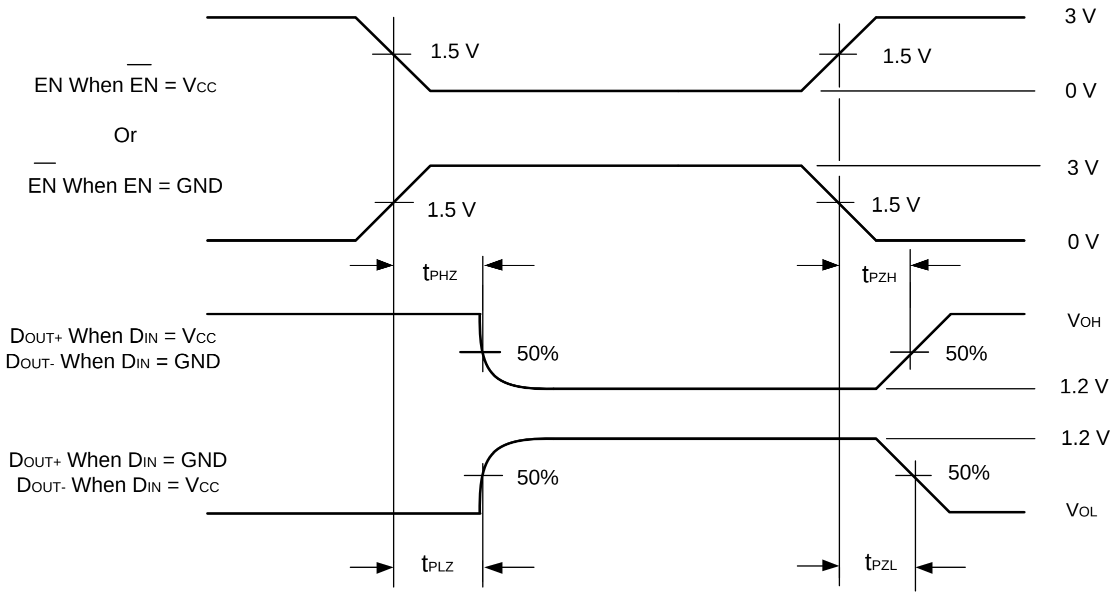


Figure 7-5. Driver TRI-STATE Delay Waveforms

8 Block diagram

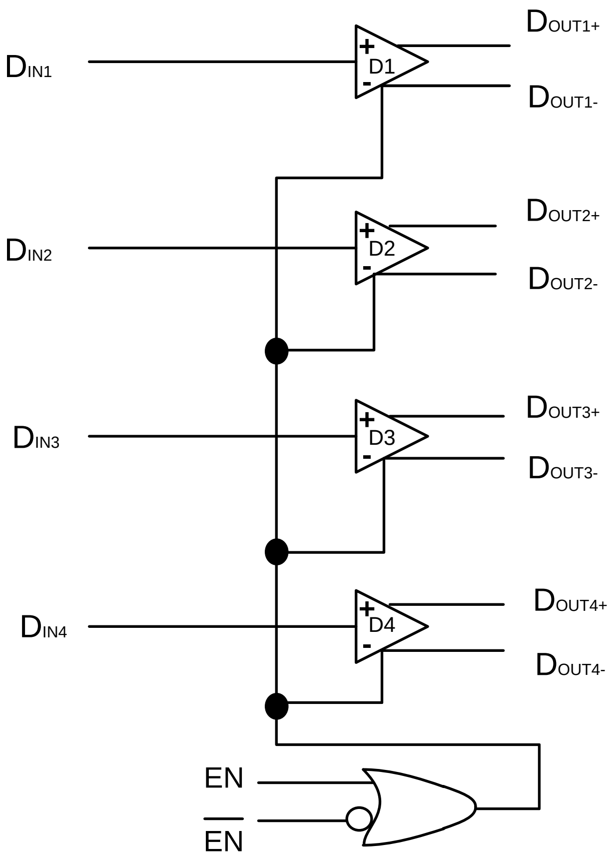


Figure 8-1. Functional Block Diagram

9 Detailed Description

9.1 Overview

LVDS drivers and receivers are intended to be primarily used in an uncomplicated point-to-point configuration as is shown in Figure 10-1. This configuration provides a clean signaling environment for the quick edge rates of the drivers. The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically, the characteristic differential impedance of the media is in the range of 100 Ω. A termination resistor of 100 Ω must be selected to match the media, and is located as close to the receiver input pins as possible. The termination resistor converts the current sourced by the driver into a voltage that is detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities as well as ground shifting, noise margin limits, and total termination loading must be considered.

The UM3404 differential line driver is a balanced current source design. A current mode driver, generally speaking has a high output impedance and supplies a constant current for a range of loads (a voltage mode driver on the other hand supplies a constant voltage for a range of loads). Current is switched through the load in one direction to produce a logic state and in the other direction to produce the other logic state. The output current is typically 3.5 mA, a minimum of 2.5 mA, and a maximum of 4.5 mA. The current mode requires (as discussed above) that a resistive termination be employed to terminate the signal and to complete the loop as shown in Figure 10-1. AC or unterminated configurations are not allowed. The 3.5-mA loop current develops a differential voltage of 350 mV across the 100-Ω termination resistor which the receiver detects with a 250-mV minimum differential noise margin neglecting resistive line losses (driven signal minus receiver threshold (350 mV – 100 mV = 250 mV)). The signal is centered around 1.2 V (Driver Offset, V_{OS}) with respect to ground as shown in Figure 9-1. Note that the steady-state voltage (V_{SS}) peak-to-peak swing is twice the differential voltage (V_{OD}) and is typically 700 mV.

The current mode driver provides substantial benefits over voltage mode drivers, such as an RS-422 driver. Its quiescent current remains relatively flat versus switching frequency. Whereas the RS-422 voltage mode driver increases exponentially in most case between 20 MHz to 50 MHz. This is due to the overlap current that flows between the rails of the device when the internal gates switch. Whereas the current mode driver switches a fixed current between its output without any substantial overlap current. This is similar to some ECL and PECL devices, but without the heavy static I_{CC} requirements of the ECL or PECL designs. LVDS requires >80% less current than similar PECL devices. AC specifications for the driver are a tenfold improvement over other existing RS-422 drivers.

The TRI-STATE function allows the driver outputs to be disabled, thus obtaining an even lower power state when the transmission of data is not required.

9.2 Fail-Safe LVDS Interface

If the LVDS link as shown in Figure 10-1 needs to support the case where the Line Driver is disabled, powered off, or removed (unplugged) and the Receiver device is powered on and enabled, the state of the LVDS bus is unknown and therefore the output state of the Receiver is also unknown. If this is of concern, consult the respective LVDS Receiver data sheet for guidance on Fail-safe Biasing options for the LVDS interface to set a known state on the inputs for these conditions.

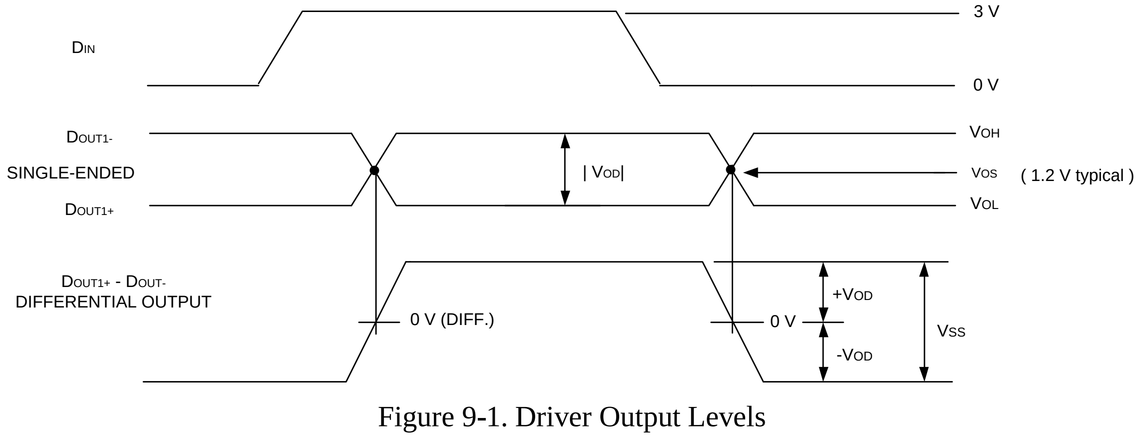


Figure 9-1. Driver Output Levels

9.3 Device Functional Modes

Table 9-1 lists the functional modes of UM3404.

Table 9-1.Truth Table

Enables		Input	Outputs	
EN	$\overline{EN}$	D_{IN}	D_{OUT+}	D_{OUT-}
L	H	X	Z	Z
All other combinations of ENABLE inputs		L	L	H
		H	H	L

10 Application Information

The UM3404 has a flow-through pinout that allows for easy PCB layout. The LVDS signals on one side of the device easily allows for matching electrical lengths of the differential pair trace lines between the driver and the receiver as well as allowing the trace lines to be close together to couple noise as common-mode. Noise isolation is achieved with the LVDS signals on one side of the device and the TTL signals on the other side.

10.1 Typical Application

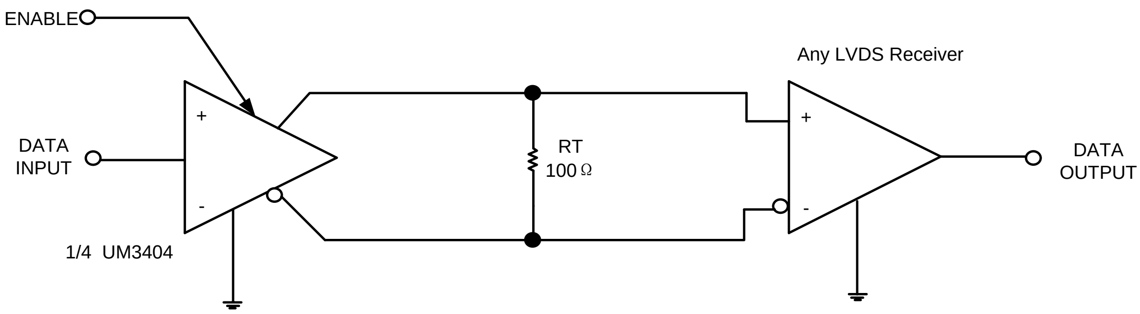


Figure 10-1. Point-to-Point Application

10.2 Design Requirements

When using LVDS devices, it is important to remember to specify controlled impedance PCB traces, cable assemblies, and connectors. All components of the transmission media must have a matched differential impedance of about 100 Ω. They must not introduce major impedance discontinuities.

Balanced cables (for example, twisted pair) are usually better than unbalanced cables (ribbon cable) for noise reduction and signal quality. Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electromagnetic radiation as common-mode (not differential mode) noise which is rejected by the LVDS receiver.

10.3 Detailed Design Procedure

10.3.1 Probing LVDS Transmission Lines

Always use high impedance (>100 kΩ), low capacitance (<2 pF) scope probes with a wide bandwidth (1 GHz)scope. Improper probing gives deceiving results.

10.3.2 Cables and Connectors, General Comments

When choosing cable and connectors for LVDS it is important to remember: Use controlled impedance media. The cables and connectors you use must have a matched differential impedance of about 100 Ω. They must not introduce major impedance discontinuities. Balanced cables (for example, twisted pair) are usually better than unbalanced cables (such as ribbon cable or simple coax) for noise reduction and signal quality. Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electromagnetic radiation as common-mode (not differential mode) noise which is rejected by the receiver. For cable distances < 0.5 m, most cables can be made to work effectively. For distances 0.5 m ≤ d ≤10 m, Category 3 (CAT 3) twisted pair cable works well, is readily available, and relatively inexpensive.

10.4 Power Supply Recommendations

Although the UM3404 draws very little power, at higher switching frequencies there is a small dynamic current component which increases the overall power consumption. The UM3404 power supply design must include local decoupling capacitance to maintain optimal device performance at higher data rates.

10.5 Layout

10.5.1 Layout Guidelines

Use at least 4 PCB layers (top to bottom): LVDS signals, ground, power, and TTL signals.

Isolate TTL signals from LVDS signals, otherwise the TTL may couple onto the LVDS lines. It is best to put TTL and LVDS signals on different layers which are isolated by power or ground plane(s).

Keep drivers and receivers as close to the (LVDS port side) connectors as possible.

10.5.2 Power Decoupling Recommendations

Bypass capacitors must be used on power pins. High frequency ceramic (surface-mount recommended) 0.1-µF in parallel with 0.01-µF, in parallel with 0.001-µF at the power supply pin as well as scattered capacitors over the printed-circuit board. Multiple vias must be used to connect the decoupling capacitors to the power planes. A 10-µF, 35-V (or greater) solid tantalum capacitor must be connected at the power entry point on the printed-circuit board.

10.5.3 Differential Traces

Use controlled impedance traces which match the differential impedance of your transmission medium (that is, cable) and termination resistor. Run the differential pair trace lines as close together as possible as soon as they leave the IC (stubs must be < 10 mm long). This helps eliminate reflections and ensure noise is coupled as common-mode. Lab experiments show that differential signals which are 1 mm apart radiate far less noise than traces 3 mm apart because magnetic field cancellation is greater with the closer traces. Plus, noise induced on the differential lines is much more likely to appear as common-mode which is rejected by the receiver.

Match electrical lengths between traces to reduce skew. Skew between the signals of a pair means a phase difference between signals which destroys the magnetic field cancellation benefits of differential signals and results in EMI. Note the velocity of propagation, v = c/Er where c (the speed of light) = 0.2997 mm/ps or 0.0118 in/ps. Do not rely solely on the auto-route function for differential traces. Carefully review dimensions to match differential impedance and provide isolation for the differential lines. Minimize the number of vias and other discontinuities on the line.

Avoid 90 °turns (these cause impedance discontinuities). Use arcs or 45 °bevels.

Within a pair of traces, the distance between the two traces must be minimized to maintain common-mode rejection of the receivers. On the printed-circuit board, this distance must remain constant to avoid discontinuities in differential impedance. Minor violations at connection points are allowable.

10.5.4 Termination

Use a resistor which best matches the differential impedance of your transmission line. The resistor must be between 90 Ω and 130 Ω. Remember that the current mode outputs need the termination resistor to generate the differential voltage. LVDS will not work without resistor termination. Typically, connect a single resistor across the pair at the receiver end.
Surface-mount 1% to 2% resistors are best. PCB stubs, component lead, and the distance from the termination to the receiver inputs must be minimized. The distance between the termination resistor and the receiver must be < 10 mm (12 mm maximum).

10.5.5 Layout Example

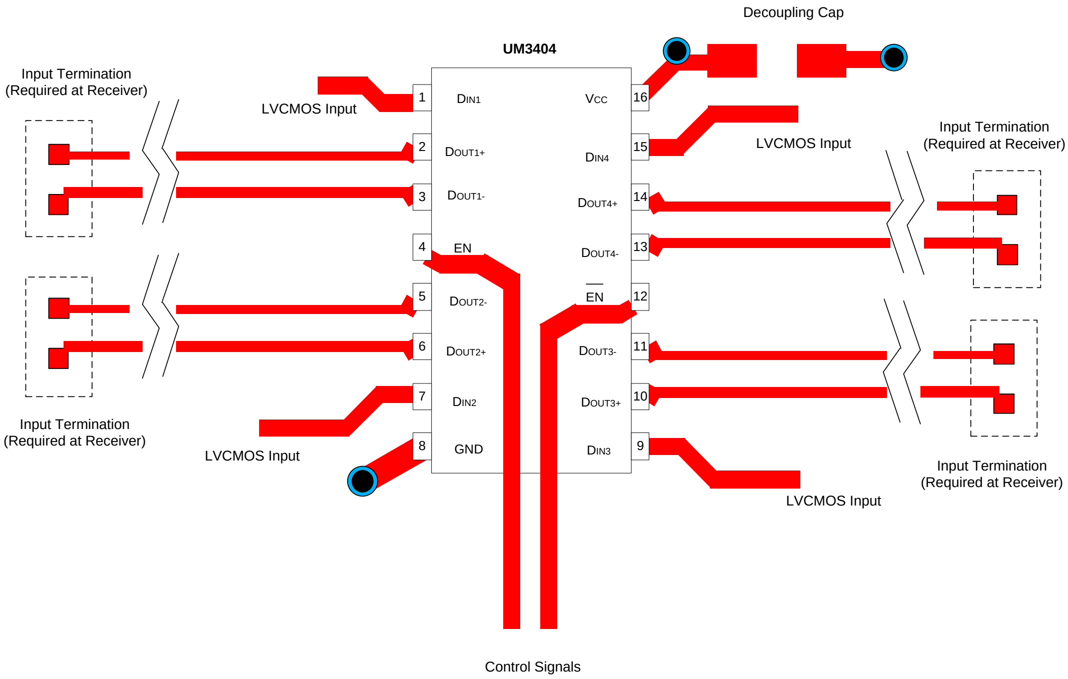
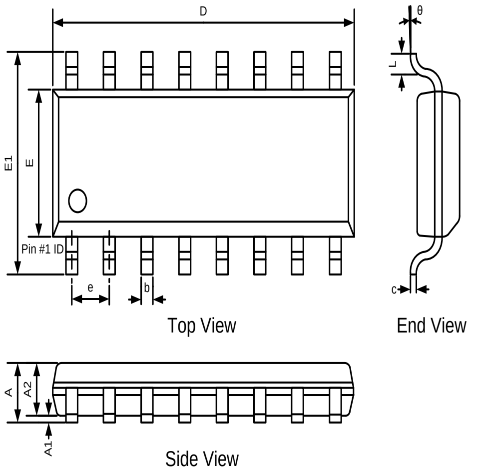


Figure 9. UM3404 Example Layout

11 Package Information

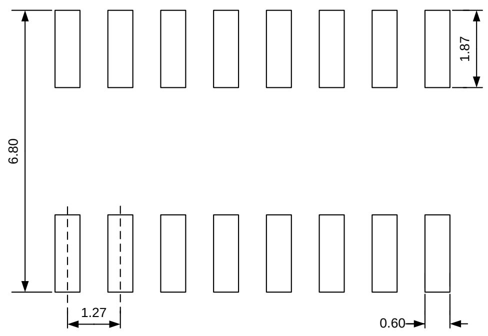
SOP16

Outline Drawing



Symbol	DIMENSIONS					
	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	1.35	1.60	1.75	0.053	0.063	0.069
A1	0.10	-	0.25	0.004	-	0.010
A2	1.25	1.45	1.65	0.049	0.057	0.065
b	0.33	-	0.51	0.013	-	0.020
c	0.17	-	0.25	0.007	-	0.010
D	9.80	10.00	10.20	0.386	0.394	0.402
E	3.80	3.90	4.00	0.150	0.154	0.157
E1	5.80	6.00	6.20	0.228	0.236	0.244
e	1.27BSC			0.050BSC		
L	0.40	-	1.27	0.016	-	0.050
θ	0 °	-	8 °	0 °	-	8 °

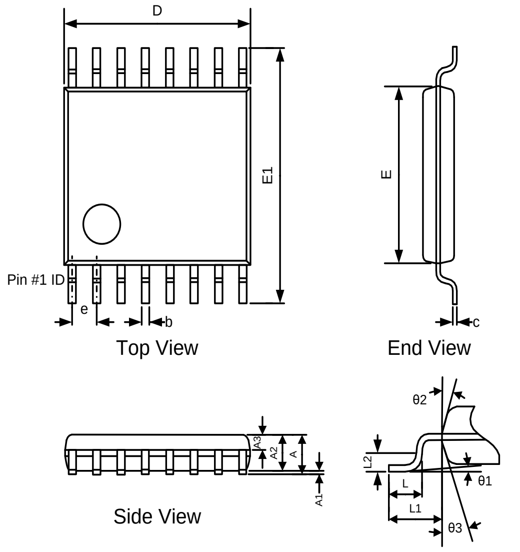
Land Pattern



NOTES:
1. Compound dimension: 7.80×4.40;
2. Unit: mm;
3. General tolerance ±0.05mm unless otherwise specified;
4. The layout is just for reference.

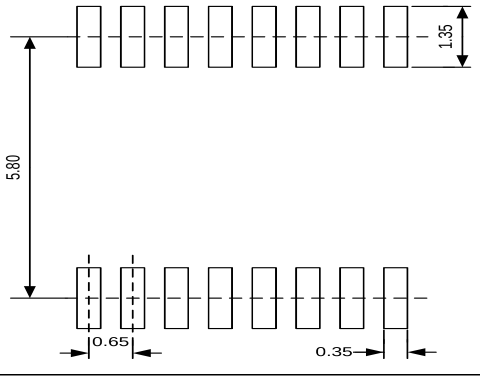
TSSOP16

Outline Drawing



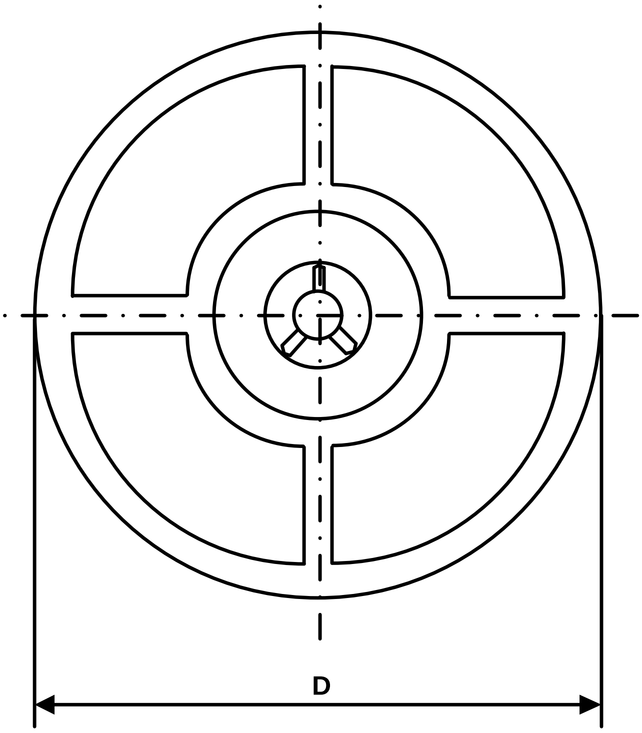
Symbol	DIMENSIONS					
	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.20	-	-	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.80	-	1.05	0.031	-	0.041
A3	0.34	0.44	0.54	0.013	0.017	0.021
b	0.19	-	0.30	0.007	-	0.012
c	0.09	-	0.20	0.004	-	0.008
D	4.86	4.96	5.10	0.191	0.195	0.201
E	4.30	4.40	4.50	0.169	0.173	0.177
E1	6.20	6.40	6.60	0.244	0.252	0.260
e	0.65BSC			0.026BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00REF			0.039REF		
L2	0.25BSC			0.010BSC		
θ1	0 °	-	8 °	0 °	-	8 °
θ2	10 °	12 °	14 °	10 °	12 °	14 °
θ3	10 °	12 °	14 °	10 °	12 °	14 °

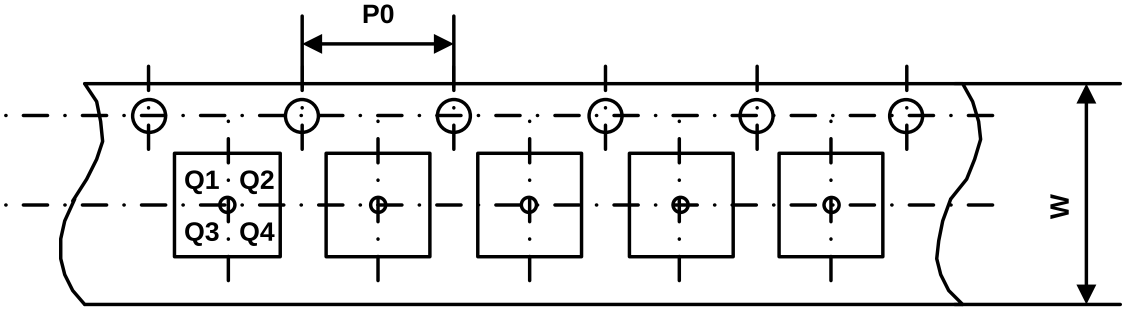
Land Pattern



NOTES:
1. Compound dimension: 7.80×4.40;
2. Unit: mm;
3. General tolerance ±0.05mm unless otherwise specified;
4. The layout is just for reference.

Packing Information





Part Number	Package Type	Carrier Width (W)	Pitch (P0)	Reel Size (D)	PIN 1 Quadrant
UM3404SG	SOP16	16 mm	4 mm	330 mm	Q1
UM3404UG	TSSOP16	16 mm	4 mm	330 mm	Q1

GREEN COMPLIANCE

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http://www.union-ic.com/index.aspx?cat_code=RoHSDeclaration

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