Low-Voltage Dual SPDT Analog Switch

UM3257 *DFN12 3.0×1.6*

General Description

The UM3257 is dual SPDT analog switch fabricated with silicon gate CMOS technology. It achieves very low propagation delay and $R_{DS(ON)}$ resistances while maintaining CMOS low power dissipation. These make it ideal for portable and battery power applications.
The switch conducts signals within power rails equally well in both directions when on, and blocks up to the power supply level when off. Break-before-make is guaranteed.
The select pin has over-voltage protection that allows voltages above V_{CC}, up to 6.5V to be present on the pin without damage or disruption of operation of the part, regardless of the operating voltage.
The UM3257 can maintain low power consumption for rail-to-rail signaling as long as the control signal input is held at a level that is greater than V_{IH} minimum and less than V_{IL} maximum by improving the control circuitry input buffer. so the part can be used in mixed voltage rail environments, especially services the mobile handset applications very well allowing for the direct interface with baseband processor general purpose I/Os, and it is no longer necessary to have the control input equal to V_{CC} to maintain low power consumption
The UM3257 is in a 12-pin, ROHS compliant, DFN12 package. It measures 3.0×1.6mm. The leads are spaced at a pitch of 0.5mm and are finished with lead free Ni-Pd. The small package makes it ideal for use in portable electronics such as cell phones, digital cameras and PDAs.

Applications

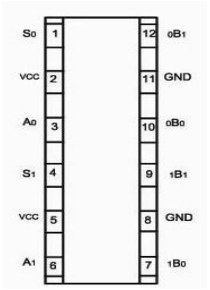
- Sample-and-Hold Circuits
- Battery-Powered Equipment
- Audio and Video Signal Routing
- Communication Circuits

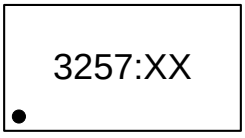
Features

- Lower I_{CC} when the S Input is within the Required V_{IH} and V_{IL} Bounds
- Low ON-State Resistance (10Ω)
- Control Inputs are 5V Tolerant
- Low Charge Injection
- Excellent ON-State Resistance Matching
- Low Total Harmonic Distortion (THD)
- 1.65V to 5.5V Single-Supply Operation
- ESD Performance:
  Human Body Model＞2kV
  Machine Model＞200V
- DFN12 Package
- Pb-Free Package

Pin Configurations

Top View





XX: Week Code
UM3257
DFN12 3.0×1.6

Ordering Information

Part Number	Packaging Type	Marking Code	Shipping Qty
UM3257	DFN12 3.0×1.6	3257	3000pcs/7 Inch Tape & Reel

Function Table

Select Input	Function
L	B0 Connected to A
H	B1 Connected to A

Absolute Maximum Ratings

Symbol	Parameter	Limit	Unit
V_{CC}	Supply Voltage	-0.5 to +6.5	V
V_{IS}	DC Switch Input Voltage (Note 1)	-0.5 to (V_{CC}+0.5)	
V_{IN}	DC IN Voltage (Note 1)	-0.5 to +6.5	
I_{IK}	DC Input Diode Current @ V_{IN}＜0V	-50	mA
I_{OUT}	DC Output Current	128	
I_{CC}/I_{GND}	DC V_{CC} or Ground Current	+100	
T_J	Junction Temperature Under Bias	+150	℃
T_{STG}	Storage Temperature	-65 to +150	
T_L	Junction Lead Temperature (Soldering, 10 Seconds)	260	
θ_{JA}	Thermal Resistance	350	℃/W
P_D	Power Dissipation @ +85℃	180	mW

Note 1: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Recommended Ratings (Note2)

Symbol	Parameter	Limit	Unit
V_{CC}	Supply Voltage Operating	1.65 to 5.5	V
V_{IS}	Switch Input Voltage	0 to V_{CC}	
V_{IN}	Select Input Voltage	0 to V_{CC}	
V_{OUT}	Output Voltage	0 to V_{CC}	
T_A	Operating Temperature	-55 to +125	℃
t_r, t_f	Input Rise and Fall Time Control Input V_{CC}=2.3V to 3.6V Control Input V_{CC}=4.5V to 5.5V	 0 to 10 0 to 5.0	ns/V

Note 2: Select input must be held HIGH or LOW, it must not float.

Electrical Characteristics

Symbol	Parameter	Test Conditions	V_{CC} (V)	Temp	Limits (–40°C to 85°C)			Unit
					Min	Typ	Max	
DC Electrical Characteristics								
	Analog Signal Range		V_{CC}	Full	0		V_{CC}	V
I_{IN}	Input Leakage Current	$0 \le V_{IN} \le 5.5V$	0 to 5.5	Room Full		±0.05	±0.1 ±1	μA
I_{OFF}	OFF State Leakage Current	$0 \le A, B \le V_{CC}$	1.65 to 5.5	Room Full		±0.05	±0.1 ±1	μA
V_{IH}	Input High Voltage		1.65 to 1.95 2.3 to 5.5	Full	0.75Vcc 0.7Vcc			V
V_{IL}	Input Low Voltage		1.65 to 1.95 2.3 to 5.5	Full			0.25Vcc 0.3Vcc	V
I_{CC}	Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_O=0$	5.5	Room Full			1.0 10	μA
R_{ON}	On-Resistance (Note3)	V_{IN}=0V, I_O=30mA V_{IN}=2.4V, I_O=-30mA V_{IN}=4.5V, I_O=-30mA	4.5	Full		3.0 5.0 7.0	6.0 8.0 13	Ω
		V_{IN}=0V, I_O=24mA V_{IN}=3V, I_O=-24mA	3.0	Full		4.0 10	8.0 19	
		V_{IN}=0V, I_O=8mA V_{IN}=2.3V, I_O=-8mA	2.3	Full		5.0 13	9.0 24	
		V_{IN}=0V, I_O=4mA V_{IN}=1.65V, I_O=-4mA	1.65	Full		6.5 17	12 39	
R_{RANGE}	On Resistance Over Signal Range (Note3, 7)	I_A=-30mA , $0 \le V_{Bn} \le Vcc$	4.5	Full			25	Ω
		I_A=-24mA, $0 \le V_{Bn} \le Vcc$	3.0	Full			50	
		I_A=-8mA, $0 \le V_{Bn} \le Vcc$	2.3	Full			100	
		I_A=-4mA, $0 \le V_{Bn} \le Vcc$	1.65	Full			300	
ΔR_{ON}	On Resistance Match Between Channels (Note3, 4, 5)	I_A=-30mA, V_{Bn} = 3.15V	4.5	Room		0.15		Ω
		I_A=-24mA, V_{Bn} = 2.1V	3.0	Room		0.2		
		I_A=-8mA, V_{Bn} = 1.6V	2.3	Room		0.5		
		I_A=-4mA, V_{Bn} = 1.15V	1.65	Room		0.5		
R_{FLAT}	On Resistance Flatness (Note3, 4, 6)	I_A=-30mA, $0 \le V_{Bn} \le Vcc$	5.0	Room		5.0		Ω
		I_A=-24mA, $0 \le V_{Bn} \le Vcc$	3.3	Room		10		
		I_A=-8mA, $0 \le V_{Bn} \le Vcc$	2.5	Room		24		
		I_A=-4mA, $0 \le V_{Bn} \le Vcc$	1.8	Room		110		

Note 3: Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B Ports).

Note 4: Parameter is characterized but not tested in production.

Note 5: $\Delta R_{ON} = | R_{ON\ (A00Bn)} - R_{ON(A11Bn)} |$ measured at identical V_{CC}, temperature and voltage levels.

Note 6: Flatness is defined as the difference between the maximum and minimum value of On Resistance over the specified range of conditions.

Note 7: Guaranteed by design.

Electrical Characteristics (Continued)

Symbol	Parameter	Test Conditions	V_{CC} (V)	Temp	Limits (–40°C to 85°C)			Unit
					Min	Typ	Max	
AC Electrical Characteristics								
t_{PHL} t_{PLH}	Propagation Delay Bus to Bus (Note 9)	V_I=OPEN	1.65 to1.95 2.3 to 2.7 3.0 to 3.6 4.5 to 5.5	Room		1.2 0.8 0.3		ns
t_{PZL} t_{PZH}	Output Enable Time Turn On Time (A to Bn)	V_I=2×V_{CC} for t_{PZL} V_I=0V for t_{PZH}	1.65 to1.95 2.3 to 2.7 3.0 to 3.6 4.5 to 5.5	Full	7.0 3.5 2.5 1.7		32 14 7.6 5.7	ns
t_{PLZ} t_{PHZ}	Output Disable Time Turn Off Time (A Port to B Port)	V_I=2×V_{CC} for t_{PLZ} V_I=0V for t_{PHZ}	1.65 to1.95 2.3 to 2.7 3.0 to 3.6 4.5 to 5.5	Full	3.0 2.0 1.5 0.8		28 15 11 8	ns
t_{BBM}	Break Before Make Time (Note 8)	R_L=50Ω, C_L=35pF	1.65 to1.95 2.3 to 2.7 3.0 to 3.6 4.5 to 5.5	Full	0.5 0.5 0.5 0.5			ns
Q_{INJ}	Charge Injection (Note 8)	C_L=0.1nF, V_{GEN}=0V, R_{GEN}=0Ω	5.0 3.3	Room		7.0 3.0		pC
O_{IRR}	Off Isolation (Note 10)	R_L=50Ω, f=10 MHz	1.65 to 5.5	Room		-55		dB
Xtalk	Crosstalk	R_L=50Ω, f=10 MHz	1.65 to 5.5	Room		-54		dB
BW	-3dB Bandwidth	R_L=50Ω	2.5 to 5.5	Room		250		MHz
THD	Total Harmonic Distortion (Note8)	R_L=600Ω, 0.5V_{P-P}, f=600Hz to 20kHz	2.5 5.0	Room		0.014 0.004		%
Capacitance								
C_{IN}	IN Pin Input Capacitance (Note11)	V_{CC}=0V				2.3		pF
C_{IO-B}	B Port Off Capacitance (Note11)	V_{CC}=5.0V				6.5		pF
C_{IOA-ON}	A Port Capacitance when Switch is Enabled (Note11)	V_{CC}=5.0V				18.5		pF

Note 8: Guaranteed by design.

Note 9: This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On Resistance of the switch and the 35 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

Note 10: Off Isolation=$20\log_{10}$ [V_A/V_{Bn}].

Note 11: T_A=+25℃, f=1MHz, Capacitance is characterized but not tested in production.

Test Circuits/Timing Diagrams

NOTE: Input driven by 50 Ω source terminated in 50 Ω
NOTE: C_L includes load and stray capacitance
NOTE: Input PRR = 1.0 MHz; t_W = 500 ns

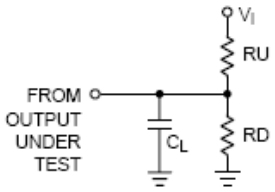
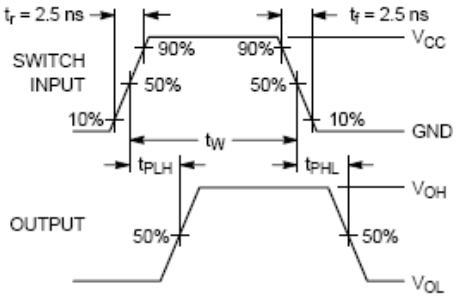


Figure 1 . AC Test Circuit



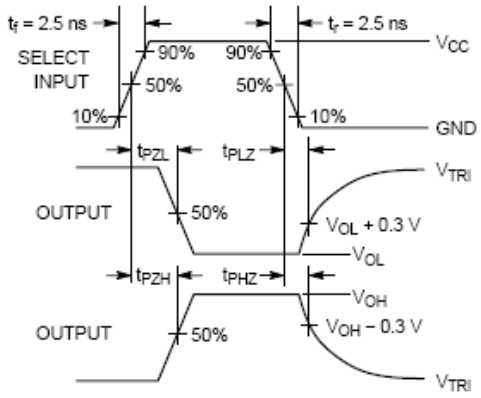
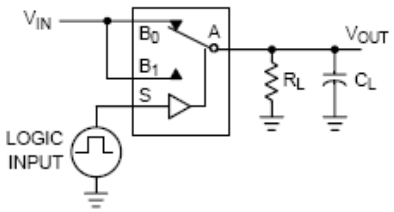


Figure 2. AC Waveforms



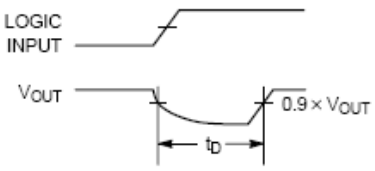


Figure 3. Break Before Make Interval Timing

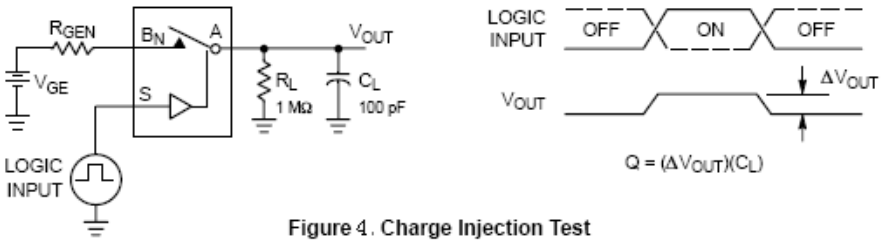


Figure 4. Charge Injection Test

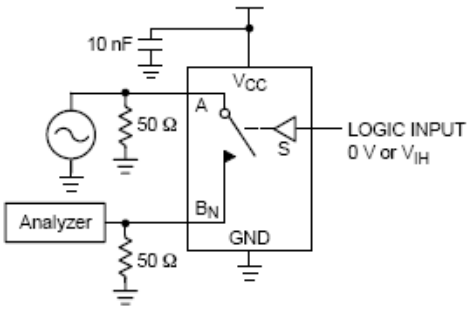


Figure 5. Off Isolation

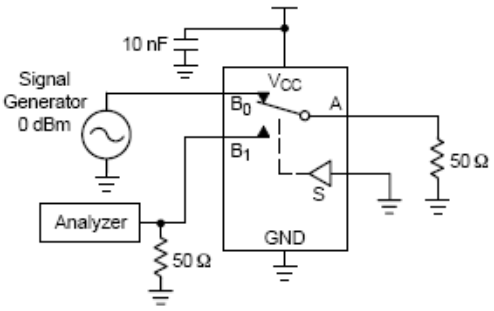


Figure 6. Crosstalk

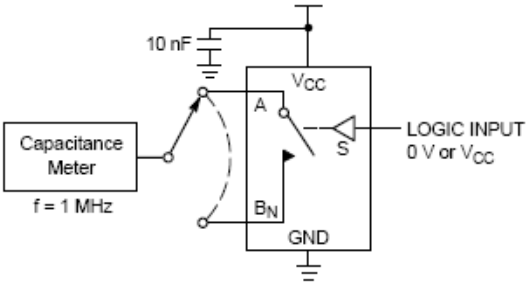


Figure 7. Channel Off Capacitance

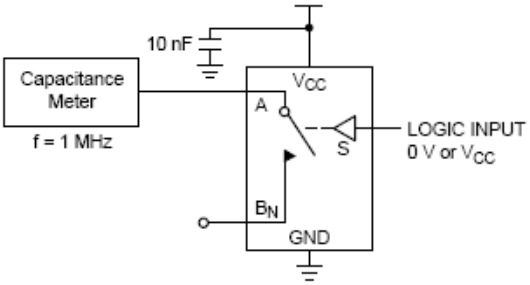


Figure 8. Channel On Capacitance

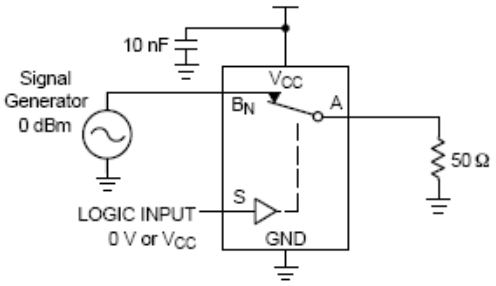
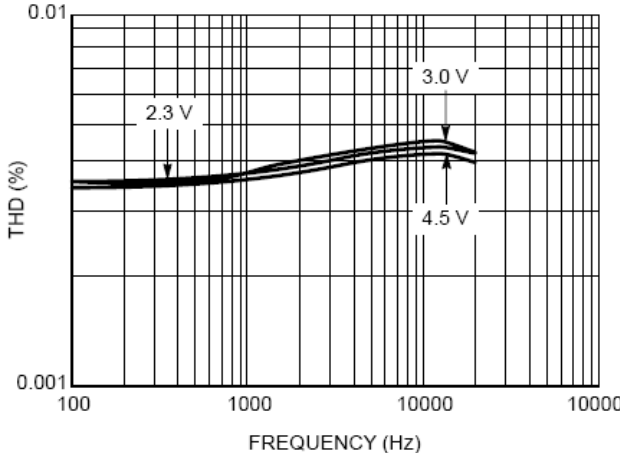


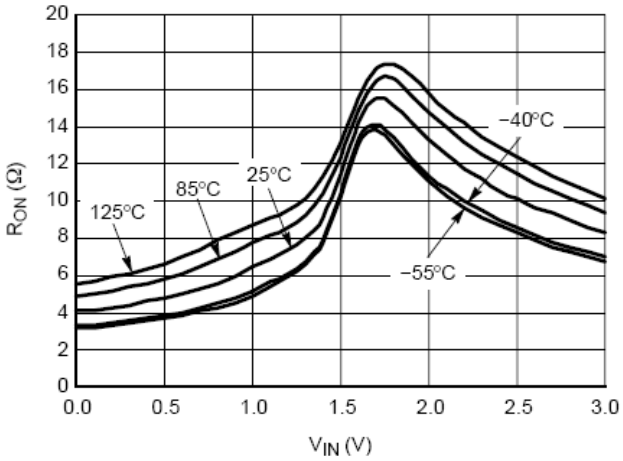
Figure 9. Bandwidth

Typical Operating Characteristics

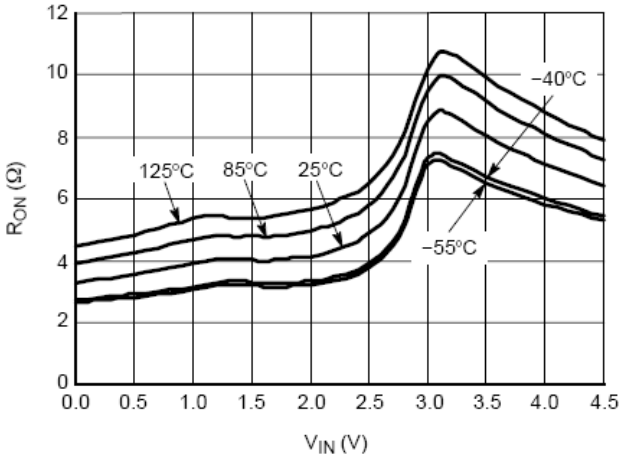
Total Harmonic Distortion vs. Frequency



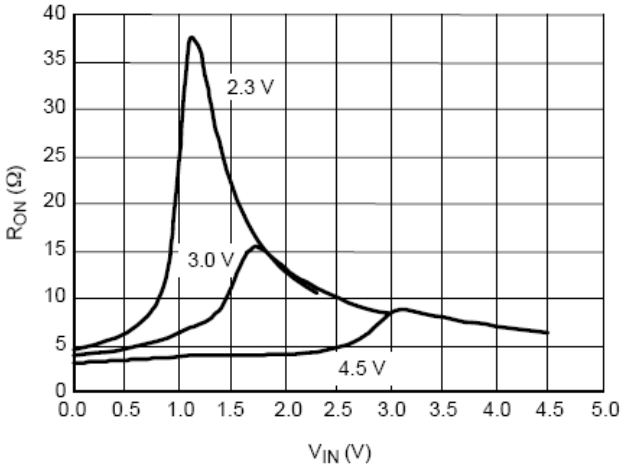
R_{ON} vs. V_{IN} vs. Temperature @ V_{CC}=3.0V



R_{ON} vs. V_{IN} vs. Temperature @ V_{CC}=4.5V

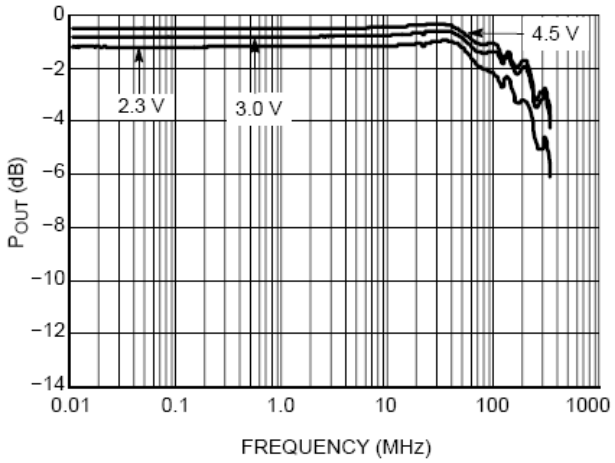


On-Resistance vs. Input Voltage

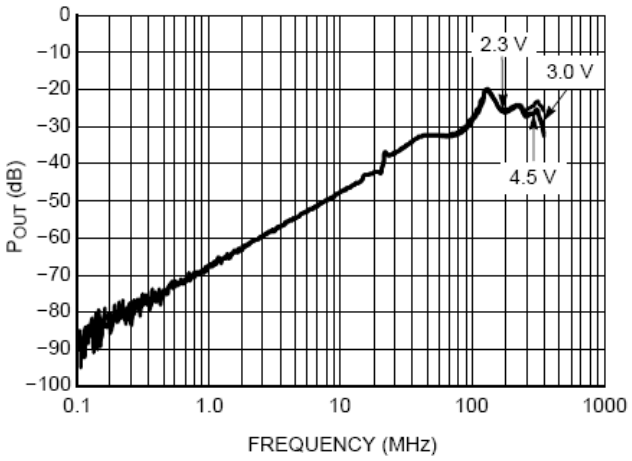


Typical Operating Characteristics (Continued)

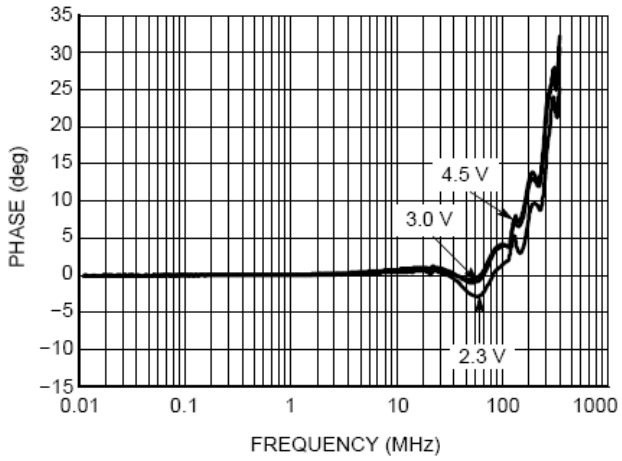
Bandwidth vs. Frequency



Off-Isolation vs. Frequency



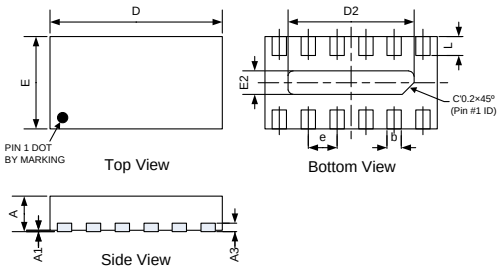
Phase Angle vs. Frequency



Package Information

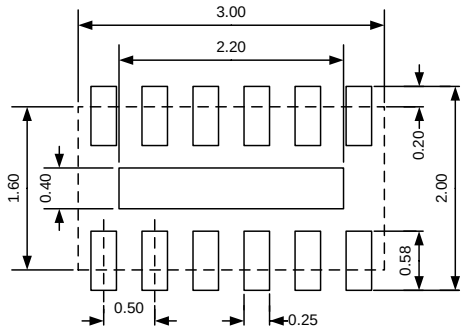
UM3257 DFN12 3.0×1.6

Outline Drawing



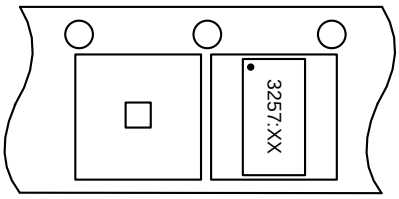
DIMENSIONS						
Symbol	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	0.50	0.55	0.605	0.020	0.022	0.024
A1	0.00	-	0.05	0.000	-	0.002
A3	0.15REF			0.006REF		
b	0.20	0.25	0.30	0.008	0.010	0.012
D	2.95	3.00	3.075	0.116	0.118	0.121
D2	2.10	2.20	2.30	0.083	0.087	0.091
E	1.55	1.60	1.675	0.061	0.063	0.066
E2	0.25	-	0.50	0.010	-	0.020
e	0.50TYP			0.020TYP		
L	0.23	-	0.38	0.009	-	0.015

Land Pattern



NOTES:
1. Compound dimension: 3.00×1.60;
2. Unit: mm;
3. General tolerance ±0.05mm unless other- wise specified;
4. The layout is just for reference.

Tape and Reel Orientation



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