

## Low-Voltage SPDT Analog Switch

### UM3157 SC70-6/SC88/SOT363

#### General Description

The UM3157 is an advanced CMOS analog switch fabricated with silicon gate CMOS technology. It achieves very low propagation delay and  $R_{DS(ON)}$  resistances while maintaining CMOS low power dissipation. These make it ideal for portable and battery power applications.

The switch conducts signals within power rails equally well in both directions when on, and blocks up to the power supply level when off. Break-before-make is guaranteed.

The select pin has over-voltage protection that allows voltages above  $V_{CC}$ , up to 6.5V to be present on the pin without damage or disruption of operation of the part, regardless of the operating voltage.

The UM3157 can maintain low power consumption for rail-to-rail signaling as long as the control signal input is held at a level that is greater than  $V_{IH}$  minimum and less than  $V_{IL}$  maximum by improving the control circuitry input buffer. so the part can be used in mixed voltage rail environments, especially services the mobile handset applications very well allowing for the direct interface with baseband processor general purpose I/Os, and it is no longer necessary to have the control input equal to  $V_{CC}$  to maintain low power consumption

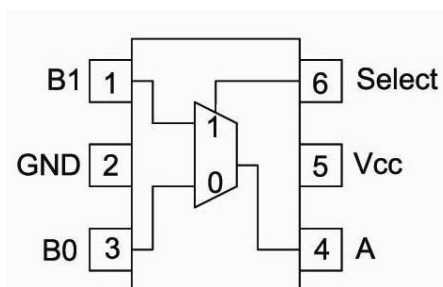
#### Applications

- Sample-and-Hold Circuits
- Battery-Powered Equipment
- Audio and Video Signal Routing
- Communication Circuits

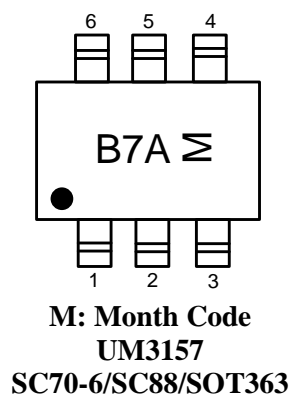
#### Features

- Control Inputs are 5V Tolerant
- Low Charge Injection
- Excellent ON-State Resistance Matching
- Low Total Harmonic Distortion (THD)
- 1.65V to 5.5V Single-Supply Operation
- ESD Performance:  
Human Body Model >2kV  
Machine Model >200V
- SC70-6/SC88/SOT363 Package
- Pb-Free Package

#### Pin Configurations



#### Top View



**Ordering Information**

Part Number	Packaging Type	Marking Code	Shipping Qty
UM3157	SC70-6/SC88/SOT363	B7A	3000pcs/7 Inch Tape & Reel

**Function Table**

Select Input	Function
L	B0 Connected to A
H	B1 Connected to A

**Absolute Maximum Ratings**

Symbol	Parameter	Limit	Unit
$V_{CC}$	Supply Voltage	-0.5 to +6.5	V
$V_S$	DC Switch Voltage (Note 1)	-0.5 to ( $V_{CC}+0.5$ )	
$V_{IN}$	DC IN Voltage (Note 1)	-0.5 to +6.5	
$I_{IK}$	DC Input Diode Current @ $V_{IN}<0V$	-50	mA
$I_{OUT}$	DC Output Current	128	
$I_{CC}/I_{GND}$	DC $V_{CC}$ or Ground Current	+100	
$T_J$	Junction Temperature Under Bias	+150	°C
$T_{STG}$	Storage Temperature	-65 to +150	
$T_L$	Junction Lead Temperature (Soldering, 10 Seconds)	260	
$\theta_{JA}$	Thermal Resistance	350	
$P_D$	Power Dissipation @ +85°C	180	mW

Note 1: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

**Recommended Ratings (Note 2)**

Symbol	Parameter	Limit	Unit
$V_{CC}$	Supply Voltage Operating	1.65 to 5.5	V
$V_{IN}$	Switch Input Voltage	0 to $V_{CC}$	
$V_{IN}$	Select Input Voltage	0 to $V_{CC}$	
$V_{OUT}$	Output Voltage	0 to $V_{CC}$	
$T_A$	Operating Temperature	-55 to +125	°C
$t_r, t_f$	Input Rise and Fall Time Control Input $V_{CC}=2.3V$ to $3.6V$ Control Input $V_{CC}=4.5V$ to $5.5V$	0 to 10 0 to 5.0	ns/V

Note 2: Select input must be held HIGH or LOW, it must not float.

**Electrical Characteristics**

Symbol	Parameter	Test Conditions	V <sub>CC</sub> (V)	Temp	Limits (-40°C to 85°C)			Unit
					Min	Typ	Max	
<b>DC Electrical Characteristics</b>								
	Analog Signal Range		V <sub>CC</sub>	Full	0		V <sub>CC</sub>	V
I <sub>IN</sub>	Input Leakage Current	0 ≤ V <sub>IN</sub> ≤ 5.5V	0 to 5.5	Room Full		±0.05	±0.1 ±1	μA
I <sub>OFF</sub>	OFF State Leakage Current	0 ≤ A, B ≤ V <sub>CC</sub>	1.65 to 5.5	Room Full		±0.05	±0.1 ±1	μA
V <sub>IH</sub>	Input High Voltage		1.65 to 2.3	Full	1.1			V
			2.3 to 2.7		1.4			
			2.7 to 3.6		1.8			
			3.6 to 4.3		2.1			
			4.3 to 5.5		2.6			
V <sub>IL</sub>	Input Low Voltage		1.65 to 2.3	Full			0.4	V
			2.3 to 2.7				0.7	
			2.7 to 3.6				1.0	
			3.6 to 4.3				1.3	
			4.3 to 5.5				1.5	
I <sub>CC</sub>	Quiescent Supply Current	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>O</sub> =0	5.5	Room Full			1.0 10	μA
R <sub>ON</sub>	On-Resistance (Note 3)	V <sub>IN</sub> =0V, I <sub>O</sub> =30mA V <sub>IN</sub> =2.4V, I <sub>O</sub> =-30mA V <sub>IN</sub> =4.5V, I <sub>O</sub> =-30mA	4.5	Full		3.0 5.0 7.0	7.0 12 15	Ω
		V <sub>IN</sub> =0V, I <sub>O</sub> =24mA V <sub>IN</sub> =3V, I <sub>O</sub> =-24mA	3.0	Full		4.0 10	9.0 20	
		V <sub>IN</sub> =0V, I <sub>O</sub> =8mA V <sub>IN</sub> =2.3V, I <sub>O</sub> =-8mA	2.3	Full		5.0 13	12 30	
		V <sub>IN</sub> =0V, I <sub>O</sub> =4mA V <sub>IN</sub> =1.65V, I <sub>O</sub> =-4mA	1.65	Full		6.5 17	20 50	
R <sub>RANGE</sub>	On Resistance Over Signal Range (Note 3, 7)	I <sub>A</sub> =-30mA 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>	4.5	Full			25	Ω
		I <sub>A</sub> =-24mA 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>	3.0	Full			50	
		I <sub>A</sub> =-8mA, 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>	2.3	Full			100	
		I <sub>A</sub> =-4mA, 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>	1.65	Full			300	
ΔR <sub>ON</sub>	On Resistance Match Between Channels (Note 3, 4, 5)	I <sub>A</sub> =-30mA, V <sub>Bn</sub> =3.15V	4.5	Room		0.15		Ω
		I <sub>A</sub> =-24mA, V <sub>Bn</sub> =2.1V	3.0	Room		0.2		
		I <sub>A</sub> =-8mA, V <sub>Bn</sub> =1.6V	2.3	Room		0.5		
		I <sub>A</sub> =-4mA, V <sub>Bn</sub> =1.15V	1.65	Room		0.5		
R <sub>FLAT</sub>	On Resistance Flatness (Note 3, 4, 6)	I <sub>A</sub> =-30mA 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>	5.0	Room		6.0		Ω
		I <sub>A</sub> =-24mA 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>	3.3	Room		12		
		I <sub>A</sub> =-8mA, 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>	2.5	Room		28		
		I <sub>A</sub> =-4mA, 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>	1.8	Room		125		

**Electrical Characteristics (Continued)**

Symbol	Parameter	Test Conditions	V <sub>CC</sub> (V)	Temp	Limits (-40°C to 85°C)			Unit
					Min	Typ	Max	
<b>AC Electrical Characteristics</b>								
t <sub>PHL</sub> t <sub>PLH</sub>	Propagation Delay Bus to Bus (Note 9)	V <sub>I</sub> =OPEN	1.65 to 1.95 2.3 to 2.7 3.0 to 3.6 4.5 to 5.5	Full			1.2 0.8 0.3	ns
t <sub>PZL</sub> t <sub>PZH</sub>	Output Enable Time Turn On Time (A to Bn)	V <sub>I</sub> =2×V <sub>CC</sub> for t <sub>PZL</sub> V <sub>I</sub> =0V for t <sub>PZH</sub>	1.65 to 1.95 2.3 to 2.7 3.0 to 3.6 4.5 to 5.5	Full	7.0 3.5 2.5 1.7		24 14 7.6 5.7	ns
t <sub>PLZ</sub> t <sub>PHZ</sub>	Output Disable Time Turn Off Time (A Port to B Port)	V <sub>I</sub> =2×V <sub>CC</sub> for t <sub>PLZ</sub> V <sub>I</sub> =0V for t <sub>PHZ</sub>	1.65 to 1.95 2.3 to 2.7 3.0 to 3.6 4.5 to 5.5	Full	3.0 2.0 1.5 0.8		13 7.5 5.3 3.8	ns
t <sub>D</sub>	Break Before Make Time (Note 8)		1.65 to 1.95 2.3 to 2.7 3.0 to 3.6 4.5 to 5.5	Full	0.5 0.5 0.5 0.5			ns
Q <sub>INJ</sub>	Charge Injection (Note 8)	C <sub>L</sub> =0.1nF, V <sub>GEN</sub> =0V, R <sub>GEN</sub> =0Ω	5.0 3.3	Room		7.0 3.0		pC
O <sub>IRR</sub>	Off Isolation (Note 10)	R <sub>L</sub> =50Ω, f=10MHz	1.65 to 5.5	Room		-57		dB
Xtalk	Crosstalk	R <sub>L</sub> =50Ω, f=10MHz	1.65 to 5.5	Room		-54		dB
BW	-3 dB Bandwidth	R <sub>L</sub> =50Ω	1.65 to 5.5	Room		250		MHz
THD	Total Harmonic Distortion (Note 8)	R <sub>L</sub> =600Ω 0.5V <sub>p-p</sub> f=600Hz to 20kHz	5.0	Room		0.011		%
<b>Capacitance</b>								
C <sub>IN</sub>	IN Pin Input Capacitance (Note 11)	V <sub>CC</sub> =0V				2.3		pF
C <sub>IO-B</sub>	B Port Off Capacitance (Note 11)	V <sub>CC</sub> =5.0V				6.5		pF
C <sub>IOA-ON</sub>	A Port Capacitance when Switch is Enabled (Note 11)	V <sub>CC</sub> =5.0V				18.5		pF

Note 3: Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B Ports).

Note 4: Parameter is characterized but not tested in production.

Note 5:  $\Delta R_{ON} = |R_{ON(B0)} - R_{ON(B1)}|$  measured at identical V<sub>CC</sub>, temperature and voltage levels.

Note 6: Flatness is defined as the difference between the maximum and minimum value of On Resistance over the specified range of conditions.

Note 7: Guaranteed by design.

Note 8: Guaranteed by design.

Note 9: This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On Resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

Note 10: Off Isolation=20log10 [V<sub>A</sub>/V<sub>Bn</sub>].

Note 11: T<sub>A</sub>=+25°C, f=1MHz, Capacitance is characterized but not tested in production.

**Test Circuits/Timing Diagrams**

NOTE: Input driven by 50 Ω source terminated in 50 Ω  
 NOTE:  $C_L$  includes load and stray capacitance  
 NOTE: Input PRR = 1.0 MHz;  $t_W = 500$  ns

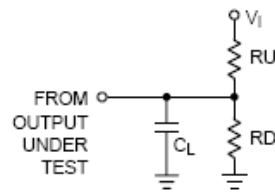


Figure 1 . AC Test Circuit

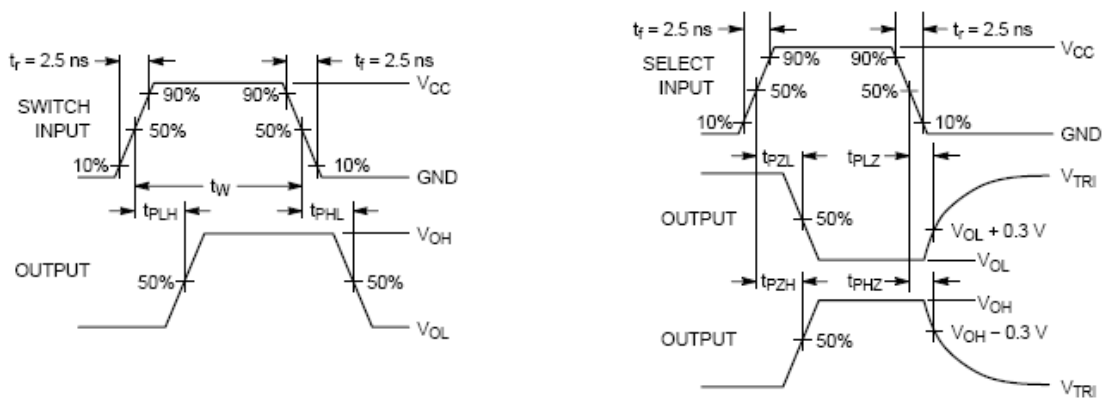


Figure 2. AC Waveforms

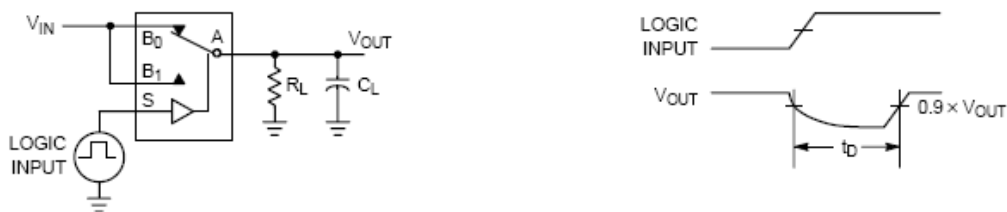


Figure 3. Break Before Make Interval Timing

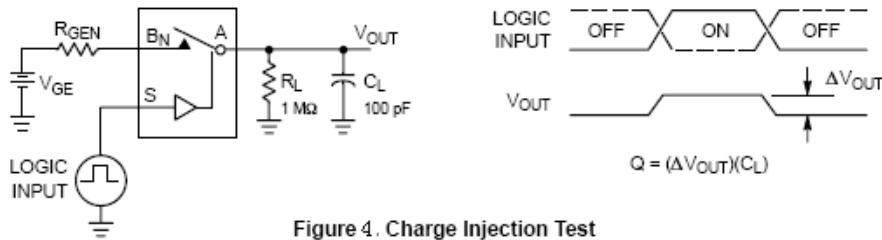


Figure 4. Charge Injection Test

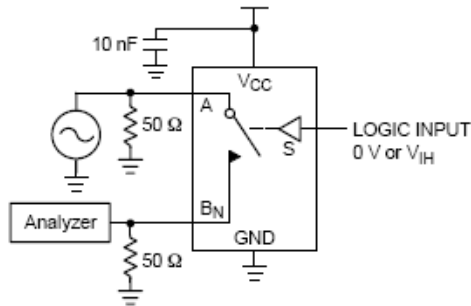


Figure 5. Off Isolation

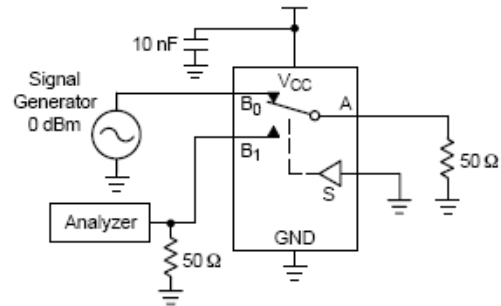


Figure 6. Crosstalk

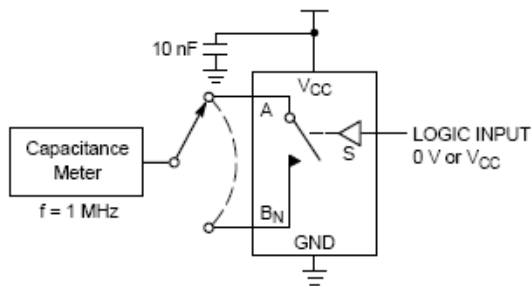


Figure 7. Channel Off Capacitance

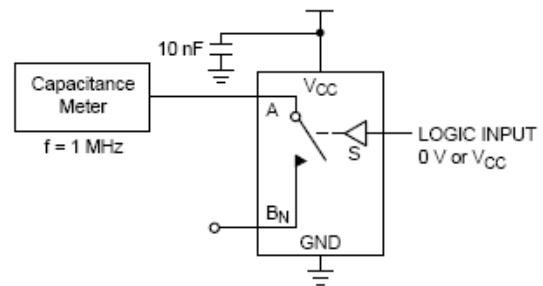


Figure 8. Channel On Capacitance

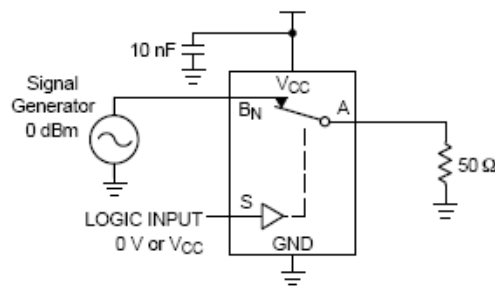
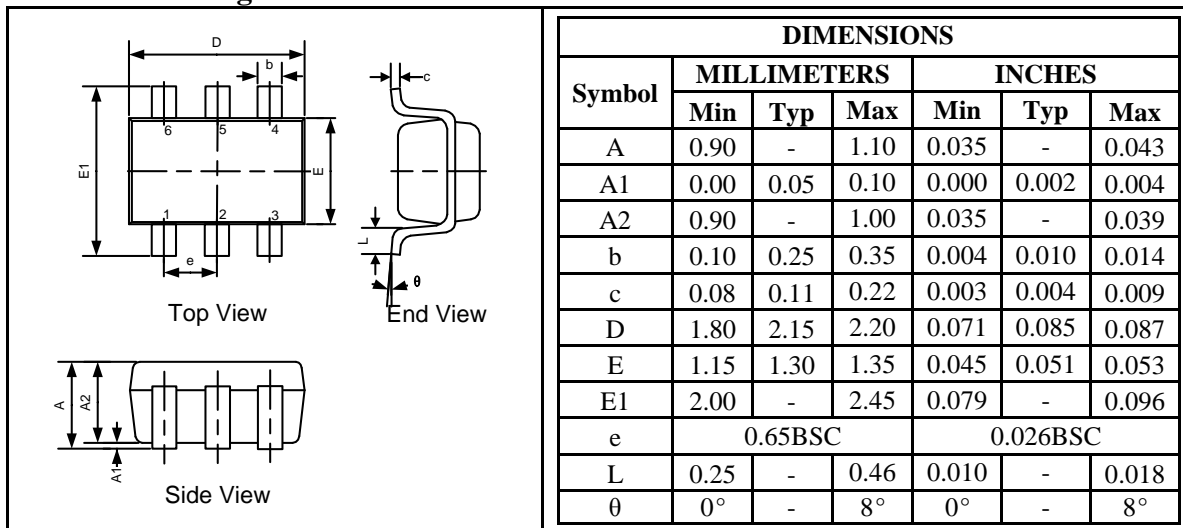


Figure 9. Bandwidth

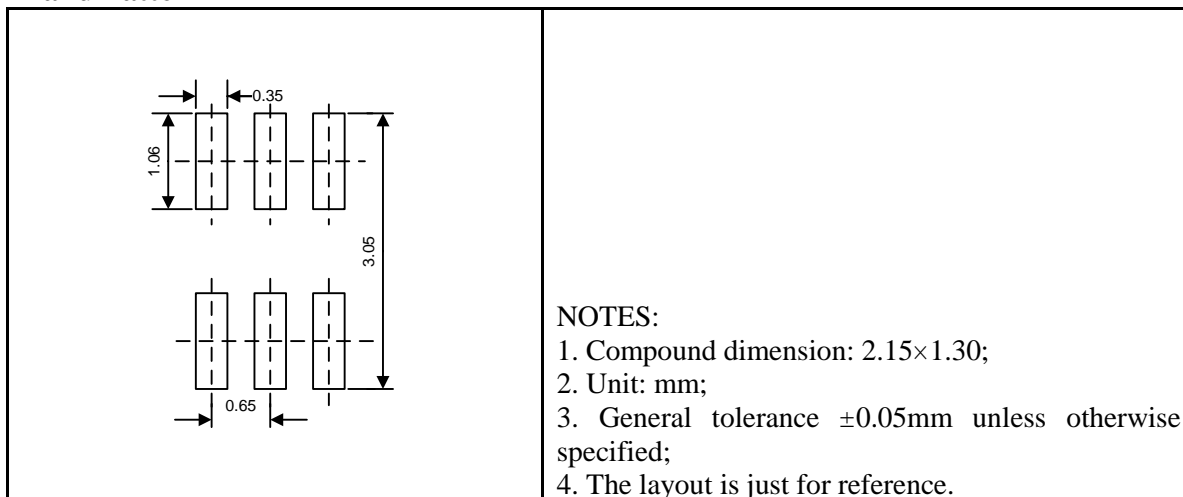
## Package Information

### UM3157 SC70-6/SC88/SOT363

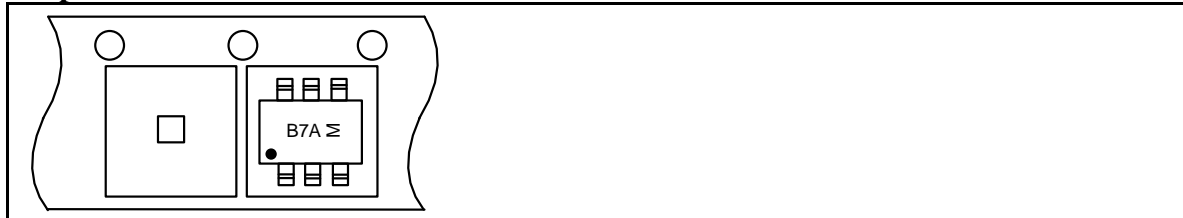
#### Outline Drawing



#### Land Pattern



#### Tape and Reel Orientation



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